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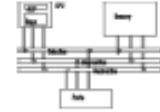


ARM ARCHITECTURE





ARM history



- 1983 developed by Acorn computers
 - To replace 6502 in BBC computers
 - 4-man VLSI design team
 - Its simplicity comes from the inexperience team
 - Match the needs for generalized SoC for reasonable power, performance and die size
 - The first commercial RISC implementation
- 1990 ARM (Advanced RISC Machine), owned by Acorn, Apple and VLSI





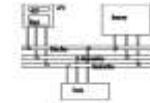
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ARM Ltd



Design and license ARM core design but not fabricate

ATAP Partners: WIN FINITY, BARCO SILEX, SOTA, DNP, Infinite Technology Corporation, SIEMENS, NSW, STEPWIND, Think, MacyoTech, COMIT SYSTEMS, YOGITECH, SIDA, SEEDS INCHI, TOPPAN, HOYA, COE, MAZ, SCIWORX, FARADAY, parthus, FLEXTRONICS, synopsys.

Tools Partners: EPI, ASHLING, CoWare, virtio, Green Hills, INNOVEDA, Computex, YOKOGAWA, ADS, Tektronix, WindRiver, Sophia systems, Axis systems, Verisity, Aptix, Agilent Technologies, Aliant, ALGATEL, COGENT, SYNOPSIS, IKOS, LAUTERBACH, cadence.

ARM in Partnership: QUALCOMM, ZTEIC, GOODRICH, ERICSSON, OKI, MOTOROLA, ADMtek, NEC, PHILIPS, TOSHIBA, intersil, AMI, EPSON, Agilent Technologies, UMC, SANYO, FUJITSU, SONY, SAMSUNG, PANASONIC, INTEL, ZEEVO, VIRA, SONY, TRISCEND, ALTEIRA, ZARLINK, ARRAYCOMM, SILICON WAVE, RESONANT, ZI CORPORATION, LIQUID AUDIO, MICROSOFT, FRONTIER, EMBLAZE, INTERTRUST, ERICSSON, GEOWORKS, US SOFTWARE, TAB SYSTEMS, OSE, AXE, SYMBIAN, MICROWARE, SUN, ETNOTEAM, WINDRIVER, MICROWARE, SUN, ETNOTEAM, ASAHICHEMICALINDUSTRYCO.LTD., SYMMETRICOM, CPS, JAVA.

RTOS Partners: Embedded Systems Products, LINUXWORKS, CMX.

Software Partners: Microsoft, Bluetooth, symbian, Dolby, Symmetricom, CPS, JAVA.





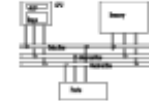
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Why ARM?



- One of the most licensed and thus widespread processor cores in the world
 - Used in PDA, cell phones, multimedia players, handheld game console, digital TV and cameras
 - ARM7: GBA, iPod
 - ARM9: NDS, PSP, Sony Ericsson, BenQ
 - ARM11: Apple iPhone, Nokia N93, N800
 - 90% of 32-bit embedded RISC processors till 2009
- Used especially in portable devices due to its low power consumption and reasonable performance





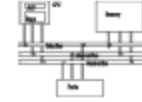
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Popular ARM architectures

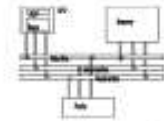


- ARM7TDMI
 - 3 pipeline stages (fetch/decode/execute)
 - High code density/low power consumption
 - One of the most used ARM-version (for low-end systems)
 - All ARM cores after ARM7TDMI include TDMI even if they do not include TDMI in their labels
- ARM9TDMI
 - Compatible with ARM7
 - 5 stages (fetch/decode/execute/memory/write)
 - Separate instruction and data cache
- ARM11





ARM family comparison



ARM family attribute comparison.

year	1995	1997	1999	2003
	ARM7	ARM9	ARM10	ARM11
Pipeline depth	three-stage	five-stage	six-stage	eight-stage
Typical MHz	80	150	260	335
mW/MHz ^a	0.06 mW/MHz	0.19 mW/MHz (+ cache)	0.5 mW/MHz (+ cache)	0.4 mW/MHz (+ cache)
MIPS ^b /MHz	0.97	1.1	1.3	1.2
Architecture	Von Neumann	Harvard	Harvard	Harvard
Multiplier	8 × 32	8 × 32	16 × 32	16 × 32

^a Watts/MHz on the same 0.13 micron process.

^b MIPS are Dhrystone VAX MIPS.





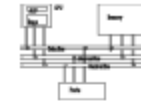
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ARM is a RISC



- RISC: simple but powerful instructions that execute within a single cycle at high clock speed.
- Four major design rules:
 - Instructions: reduced set/single cycle/fixed length
 - Pipeline: decode in one stage/no need for microcode
 - Registers: a large set of general-purpose registers
 - Load/store architecture: data processing instructions apply to registers only; load/store to transfer data from memory
- Results in simple design and fast clock rate
- The distinction blurs because CISC implements RISC concepts





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ARM features



- Different from pure RISC in several ways:
 - Variable cycle execution for certain instructions: multiple-register load/store (faster/higher code density)
 - Inline barrel shifter leading to more complex instructions: improves performance and code density
 - Thumb 16-bit instruction set: 30% code density improvement
 - Conditional execution: improve performance and code density by reducing branch
 - Enhanced instructions: DSP instructions





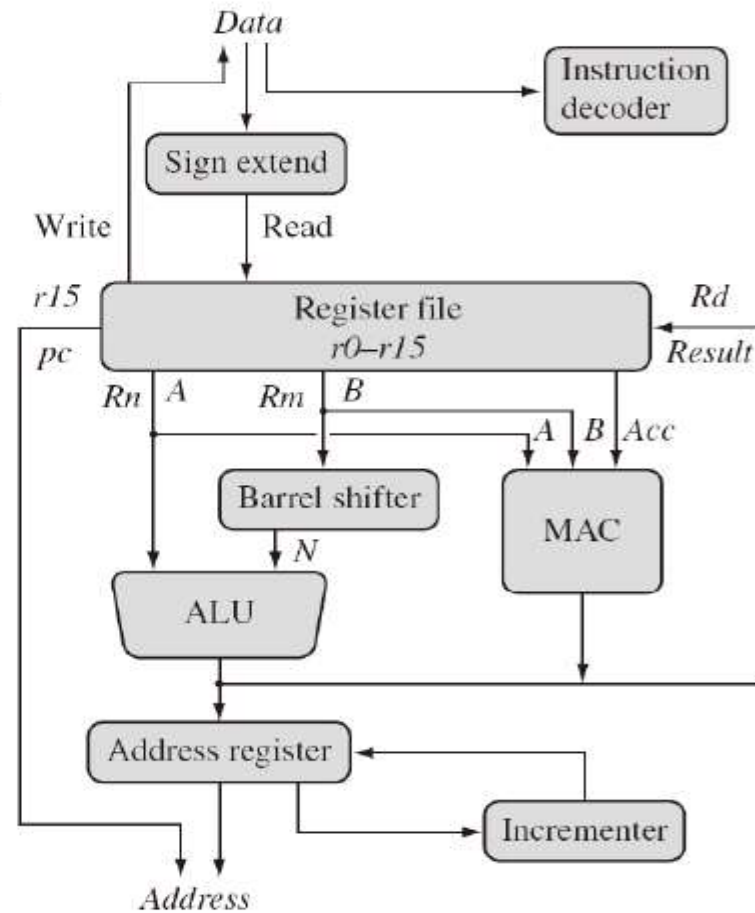
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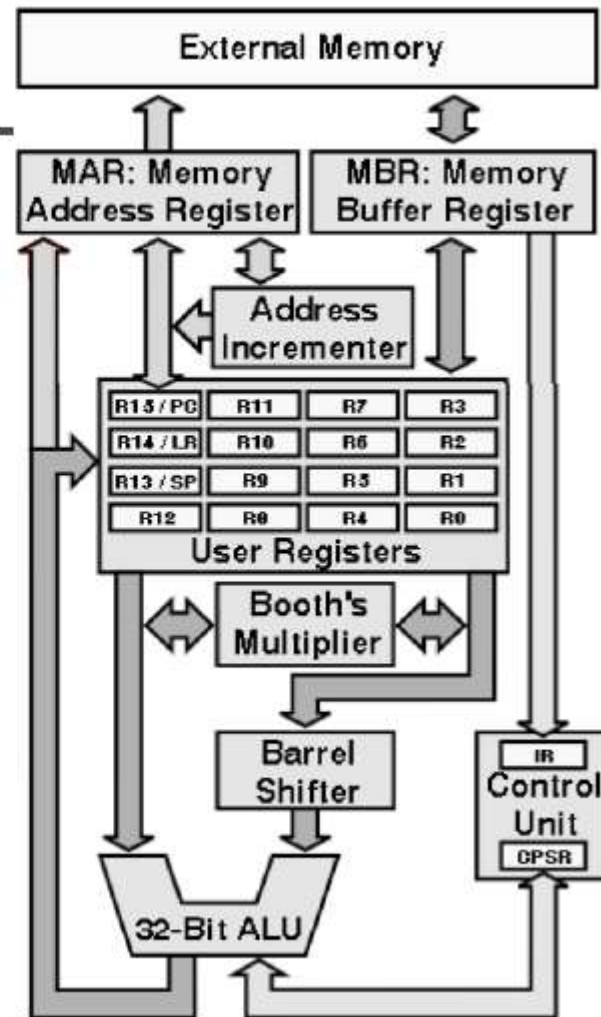
ARM architecture





ARM architecture

- Load/store architecture
- A large array of uniform registers
- Fixed-length 32-bit instructions
- 3-address instructions





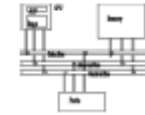
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Registers

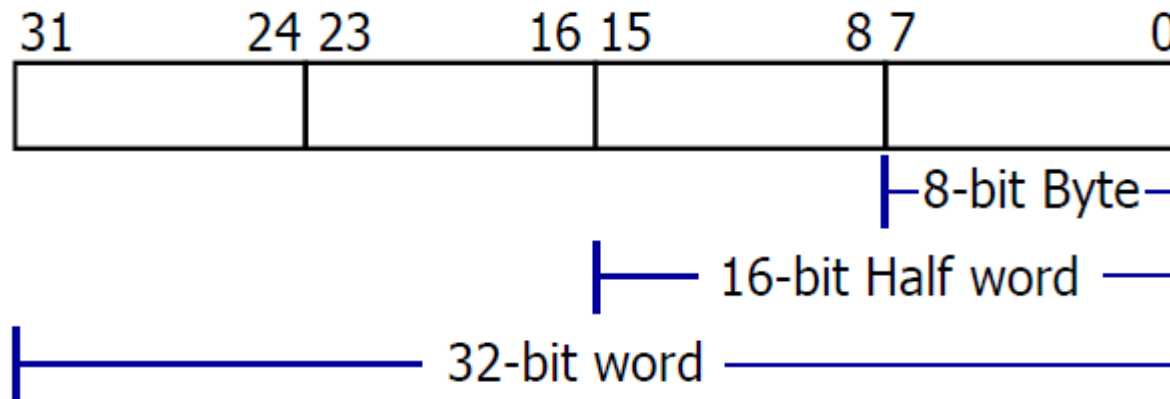
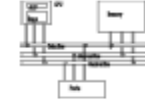


- Only 16 registers are visible to a specific mode.
A mode could access
 - A particular set of r0-r12
 - r13 (sp, stack pointer)
 - r14 (lr, link register)
 - r15 (pc, program counter)
 - Current program status register (cpsr)
 - The uses of r0-r13 are orthogonal





General-purpose registers

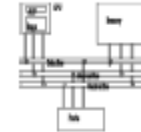


- 6 data types (signed/unsigned)
- All ARM operations are 32-bit. Shorter data types are only supported by data transfer operations.





Program counter



- Store the address of the instruction to be executed
- All instructions are 32-bit wide and word-aligned
- Thus, the last two bits of pc are undefined.





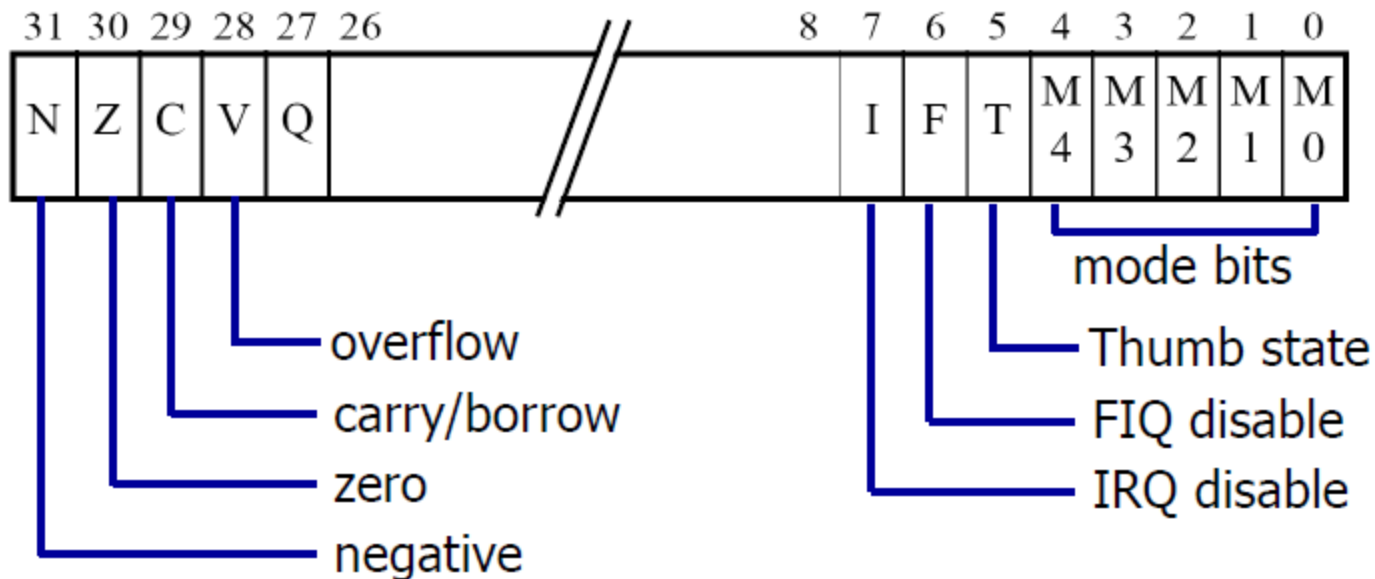
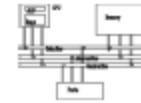
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Program status register (CPSR)





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Processor modes



Processor mode		Description
User	usr	Normal program execution mode
FIQ	fiq	Supports a high-speed data transfer or channel process
IRQ	irq	Used for general-purpose interrupt handling
Supervisor	svc	A protected mode for the operating system
Abort	abt	Implements virtual memory and/or memory protection
Undefined	und	Supports software emulation of hardware coprocessors
System	sys	Runs privileged operating system tasks





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Register organization

