SNS COLLEGE OF ENGINEERING

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An Autonomous Institution

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UNIT 2
Parallel communication Interface

8255A - Programmable Peripheral Interface

- The 8255A is a general purpose programmable I/O device designed to transfer the data from I/O to interrupt I/O under certain conditions as required.
- It can be used with almost any microprocessor. It consists of three 8-bit bidirectional I/O ports (24I/O lines) which can be configured as per the requirement.

8255A has three ports

PORT A

PORT B

PORT C

Port A and **Port B** are 8 bit parallel ports.

Port C can be split into two parts, i.e. PORT C lower (PC0-PC3) and PORT C upper (PC7-PC4) by the control

These three ports are further divided into two groups,

i.e. Group A includes PORT A and upper PORT C.

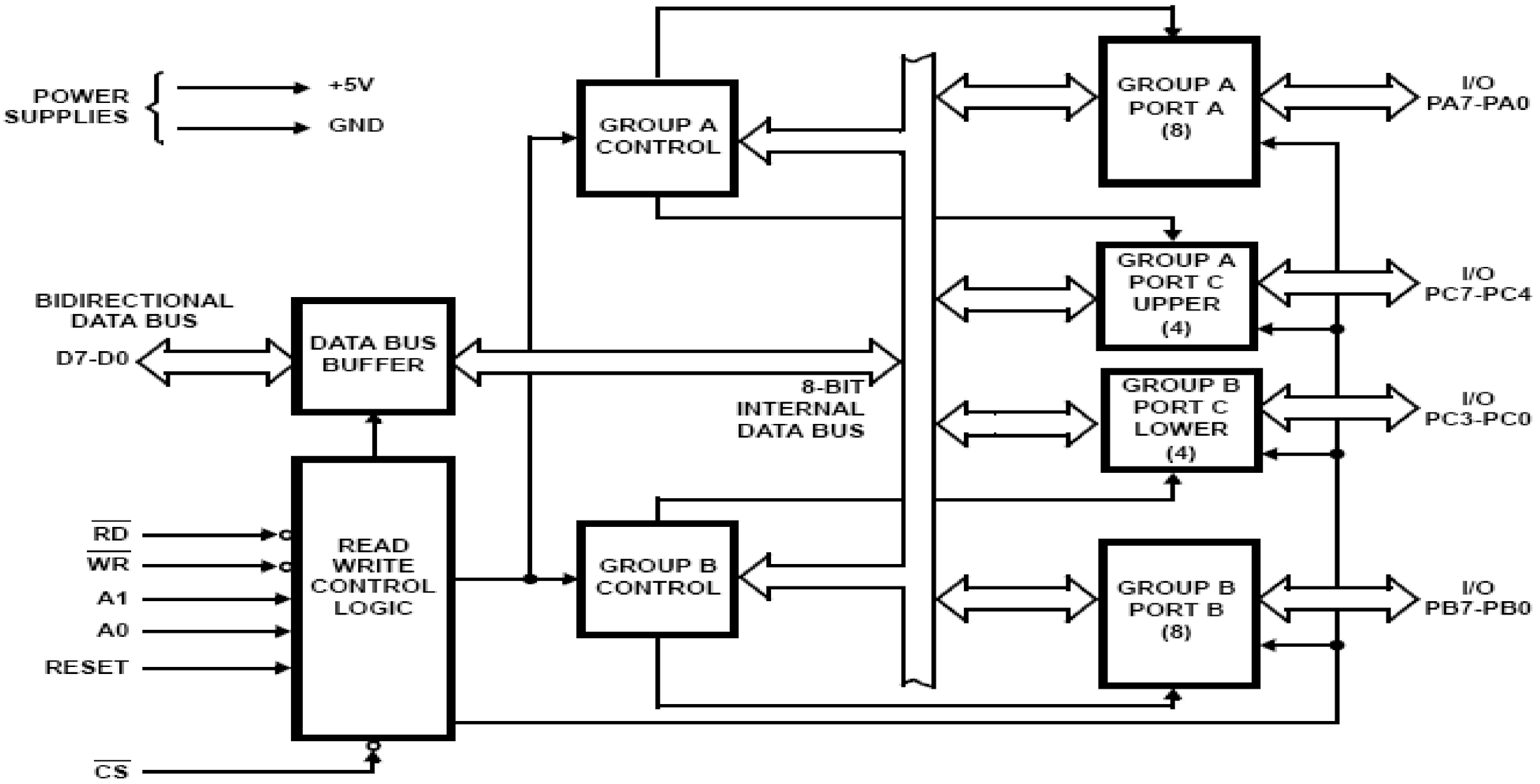
Group B includes PORT B and lower PORT C

These two groups can be programmed in three different modes

Three operating modes :

Mode-0(simple I/O port)
Mode-1(Handshake I/O port)
Mode-2(Bidirectional I/O port)

Block Diagram-8255



Mode 0

In this mode, Port A and B is used as two 8-bit ports and Port C as two 4-bit ports.

Each port can be programmed in either input mode or output mode where outputs are latched and inputs are not latched.

Ports do not have interrupt capability.

Ports in mode 0 is used to interfaces LEDs, Hexa keypad and 7 segment LEDS to the processor.

Mode 1

In this mode, Port A and B is used as 8-bit I/O ports.

They can be configured as either input or output ports.

Each port uses three lines from port C as handshake signals.

Inputs and outputs are latched

MODE 1 :(Input/output with Hand shake)

In this mode, input or output is transferred by hand shaking Signals.

Handshaking signals is used to transfer data between whose data transfer is not same.

Mode 2

In this mode, Port A can be configured as the bidirectional port and Port B either in Mode 0 or Mode 1.

Port A uses five signals from Port C as handshake signals for data transfer.

The remaining three signals from Port C can be used either as simple I/O or as handshake for port B.

Mode 2

MODE 2:bi-directional I/O data transfer:

This mode allows bidirectional data transfer over a single 8-bit data bus using handshake signals.

This feature is possible only Group A

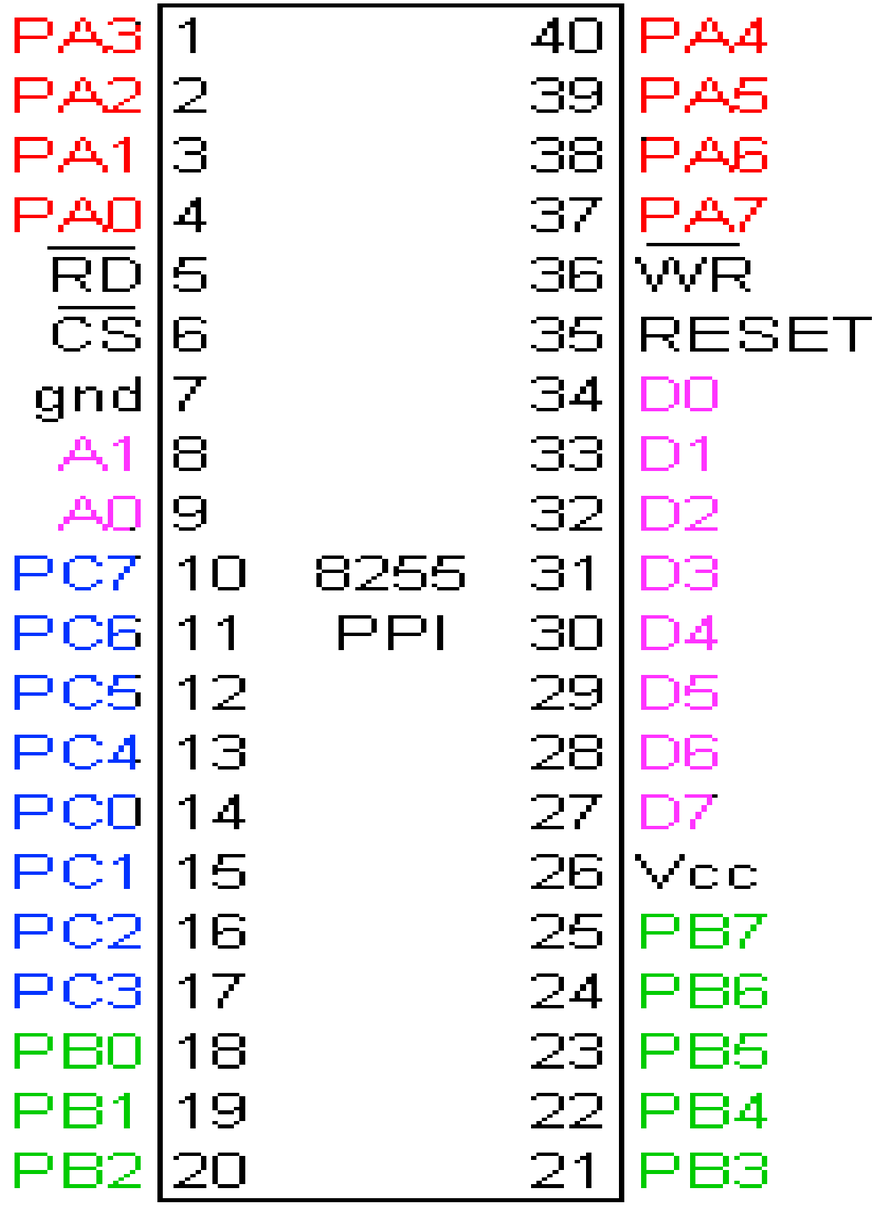
Port A is working as 8-bit bidirectional.

PC3-PC7 is used for handshaking purpose.

The data is sent by CPU through this port , when the peripheral request it.

CONTROL WORD FORMATS:

In the INPUT mode , When RESET is High all 24 pins (3-ports) be a input mode.


PA3 1
PA2 2
PA1 3
PA0 4
RD 5
CS 6
gnd 7
A1 8
A0 9
PC7 10
PC6 11
PC5 12
PC4 13
PC0 14
PC1 15
PC2 16
PC3 17
PB0 18
PB1 19
PB2 20
8255
PPI
40 PA4
39 PA5
38 PA6
37 PA7
36 WR
35 RESET
34 D0
33 D1
32 D2
31 D3
30 D4
29 D5
28 D6
27 D7
26 Vcc
25 PB7
24 PB6
23 PB5
22 PB4
21 PB3

Function of pins:
Data bus(D_0-D_7):These are 8-bit bi-directional buses, connected to 8086 data bus for transferring data.

CS: This is Active Low signal. It stands for Chip Select. A LOW on this input selects the chip and enables the communication between the 8255 and the CPU.

Read: This is Active Low signal, when it is Low the microprocessor reads data from a selected I/O port of 8255A.

Write: This is Active Low signal, when it is Low the microprocessor writes data into a selected I/O port .

Address (A_0-A_1):This is used to select the ports.
RESET: This is used to reset the device. That means clear control registers.

PA_0-PA_7:It is the 8-bit bi-directional I/O pins used to send the data to peripheral or to receive the data from peripheral.

PB_0-PB_7:Similar to PA

PC_0-PC_7:This is also 8-bit bidirectional I/O pins. These lines are divided into two groups.

1. PC_0 to PC_3(Lower Groups)
2. PC_4 to PC_7 (Higher groups)

These two groups working in separately using 4 data's.

Data Bus buffer:
It is a 8-bit bidirectional Data bus.

Used to interface between 8255 data bus with system bus.

The internal data bus and Outer pins D_0-D_7 pins are connected in internally.

The direction of data buffer is decided by Read/Control Logic.

Read/Write Control Logic:

This is getting the input signals from control bus and Address bus

Control signal are RD and WR.

Address signals are A0,A1,and CS.

8255 operation is enabled or disabled by CS.

Group A and Group B control:

Group A and B get the Control Signal from CPU and send the command to the individual control blocks.

- Group A send the control signal to port A and Port C (Upper) PC_7-PC_4.
- Group B send the control signal to port B and Port C (Lower) PC_3-PC_0.
- PORT A:
- This is a 8-bit buffered I/O latch.
- It can be programmed by mode 0 , mode 1, mode 2 .
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PORT B:

This is a 8-bit buffer I/O latch.

It can be programmed by mode 0 and mode 1.

PORT C:

This is a 8-bit Unlatched buffer Input and an Output latch.

It is splitted into two parts.

It can be programmed by bit set/reset operation.

Operation modes in 8255

Two operating modes:

I/O mode(mode 0, mode 1, mode2)

Bit set/Reset mode

BIT SET/RESET MODE:

The PORT C can be Set or Reset by sending OUT instruction to the CONTROL registers.

I/O MODES:

MODE 0(Simple input / Output):

In this mode , port A, port B and port C is used as individually (Simply).

Features:

Outputs are latched , Inputs are buffered not latched.

Ports do not have Handshake or interrupt capability.

Control words

Two control words:

I/O mode set control word(MSW)

Bit set/reset control word(BSR)

MSW is used to specify I/O functions.

BSR is used to set/reset individual pins of Port C.

Both the control words are written in the same control register.

PORT B:

This is a 8-bit buffer I/O latch.

It can be programmed by mode 0 and mode 1.

PORT C:

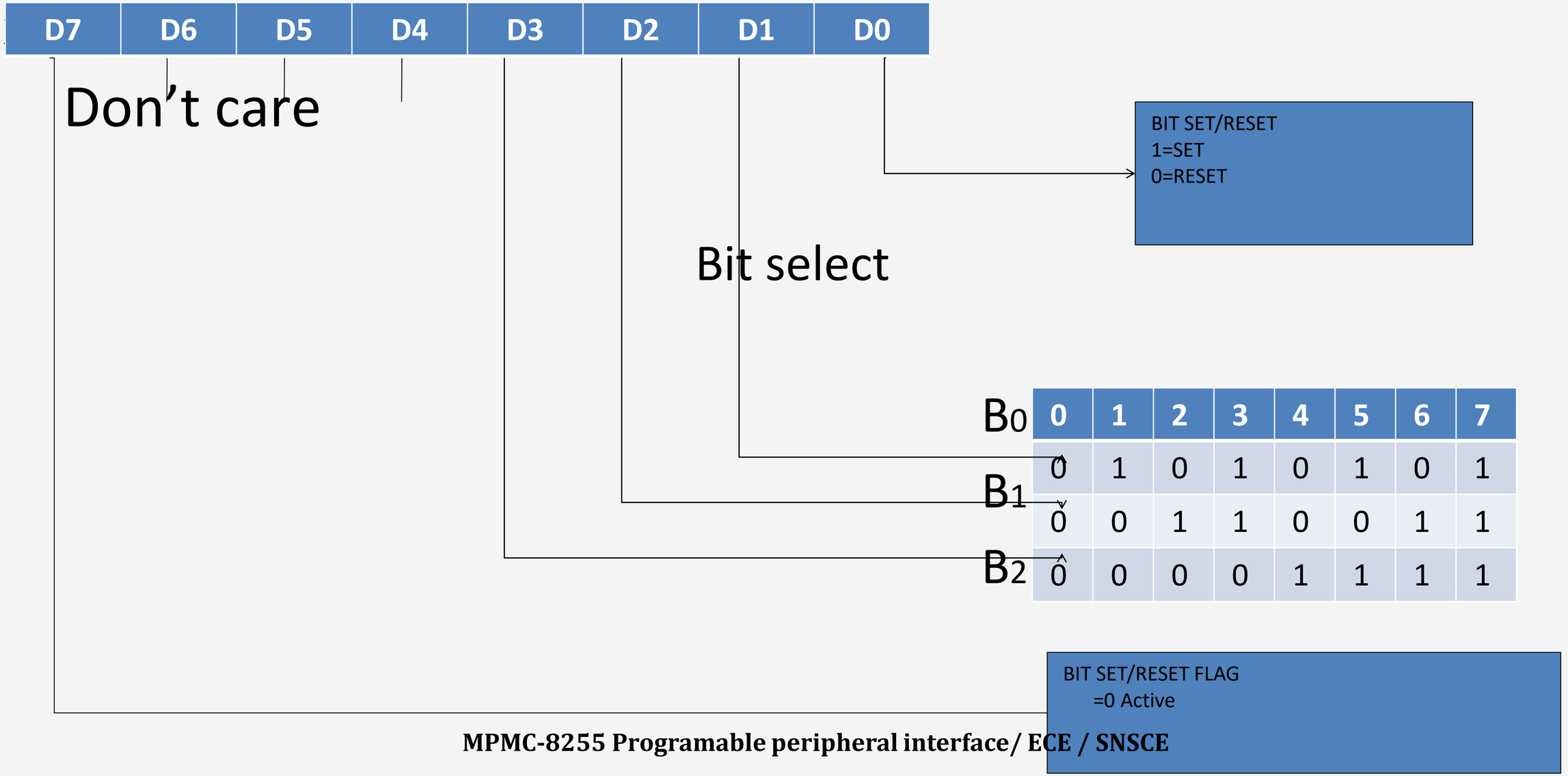
This is a 8-bit Unlatched buffer Input and an Output latch.

It is splitted into two parts.

It can be programmed by bit set/reset operation.

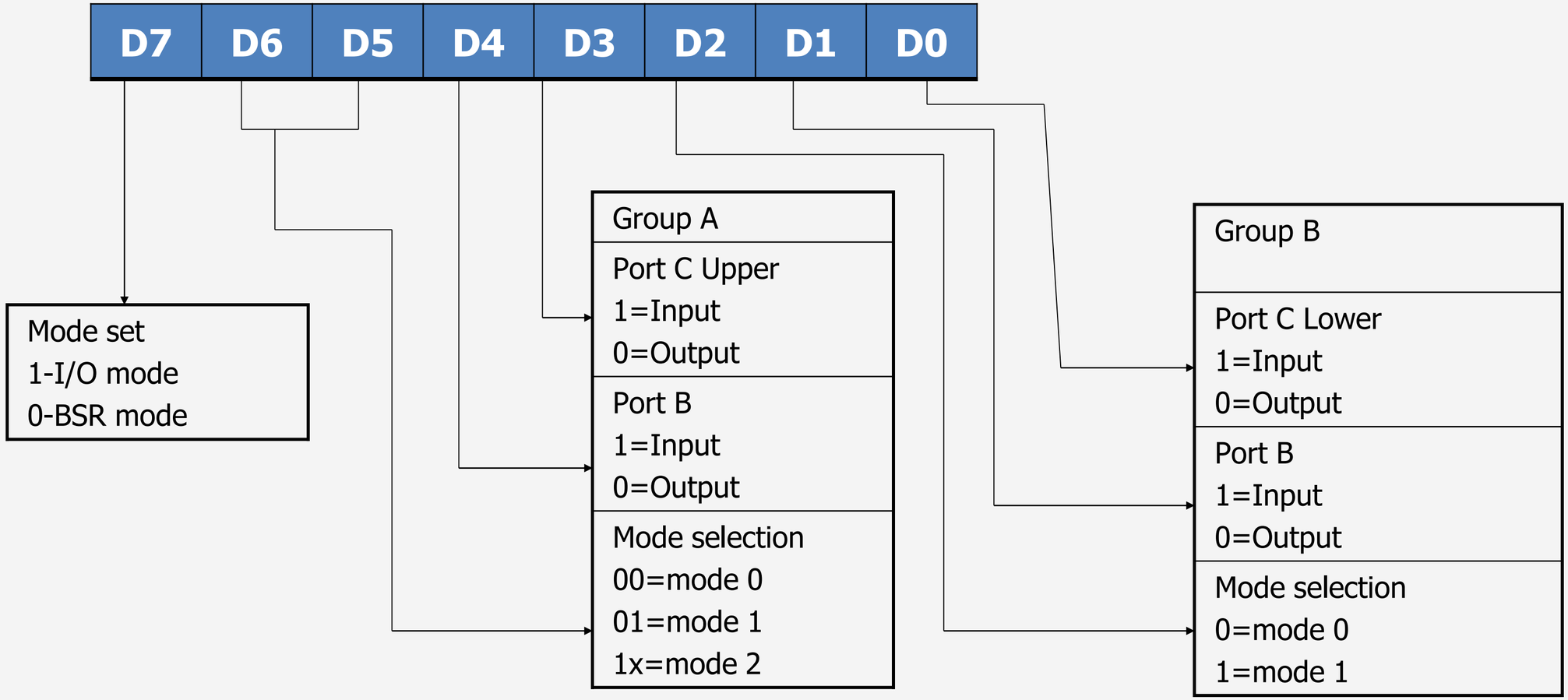
FOR BIT SET/RESET MODE:

- This is bit set/reset control word format.



FORMAT OF I/O MODE:

The mode format for I/O as shown in figure



The control word for both mode is same.

Bit D7 is used for specifying whether word loaded in to

Bit set/reset mode or Mode definition word.

D7=1=Mode definition mode.

D7=0=Bit set/Reset mode.

Assessment

What is Interfacing?

What is the use of parallel communication Interfacing

THANK YOU