SNS COLLEGE OF ENGINEERING
(Autonomous)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MICROPROCEESORS & ADVANCED MICRO CONTROLLERS

DSP PROCESSOR

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DSP - ARCHITECTURE

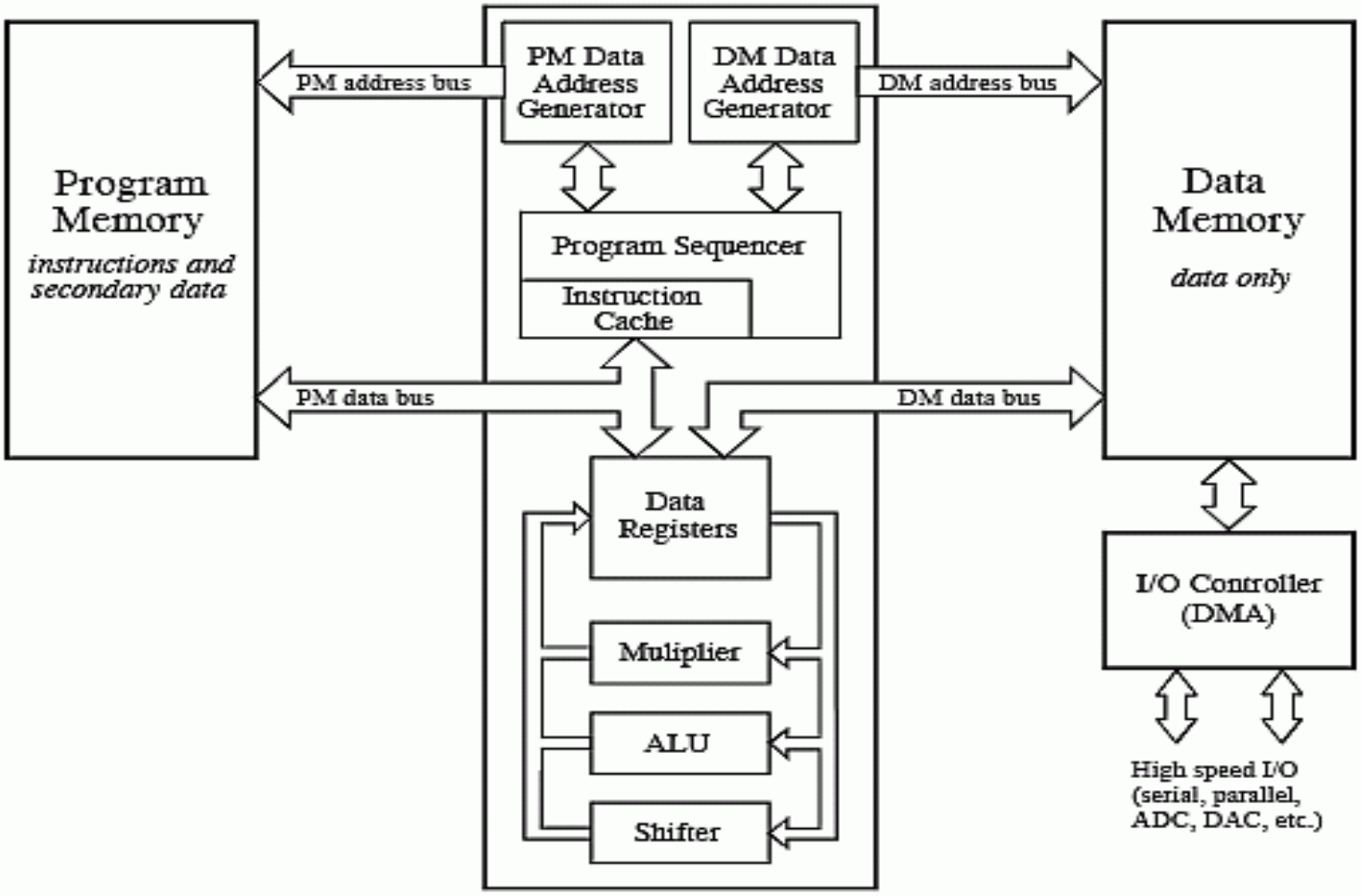


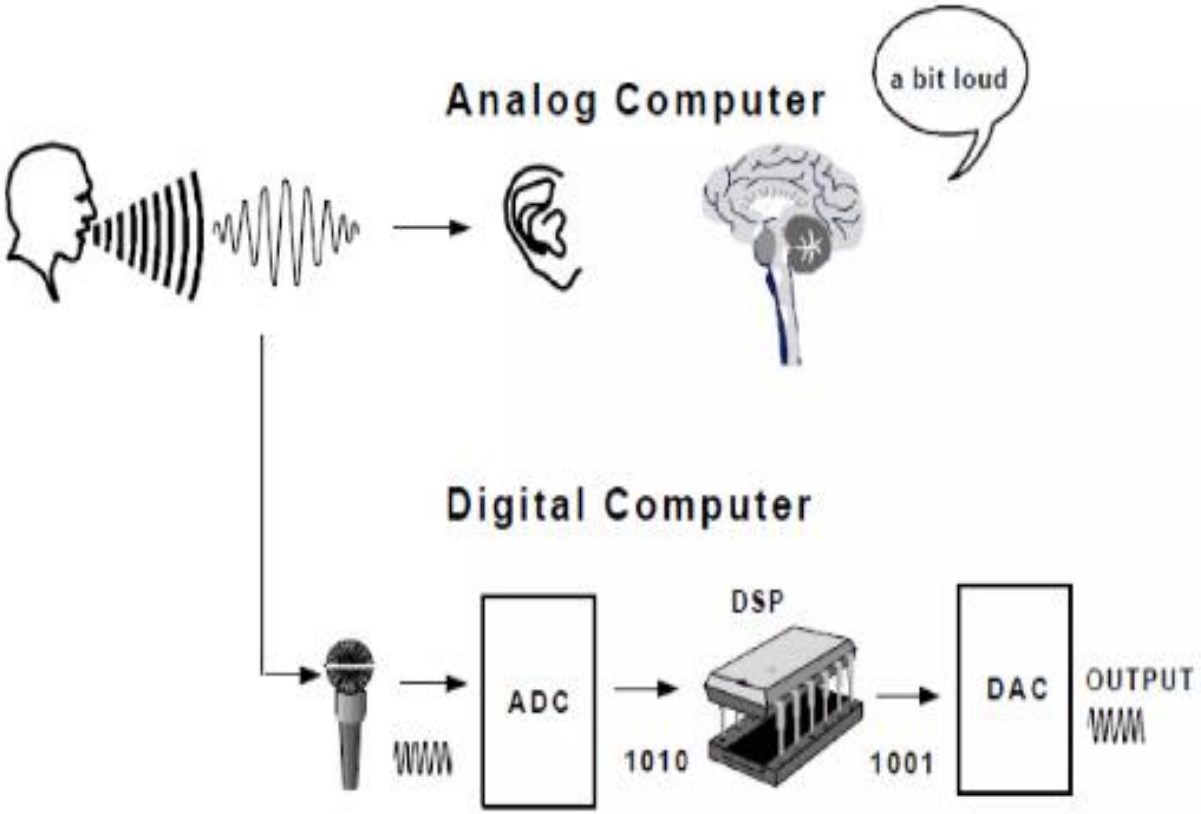
FIGURE 28-5
Typical DSP architecture. Digital Signal Processors are designed to implement tasks in parallel. This simplified diagram is of the Analog Devices SHARC DSP. Compare this architecture with the tasks needed to implement an FIR filter, as listed in Table 28-1. All of the steps within the loop can be executed in a single clock cycle.

INTRODUCTION

A digital signal processor (DSP) is an integrated circuit designed for high-speed data manipulations, and is used in

- Audio
- Communications
- image manipulation
- Other data-acquisition and
- Data-control applications.

How Analog and Digital Signals Work Together

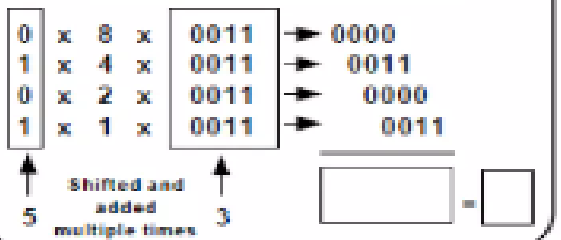


Why Do We Need Digital Signal Processors?

Add 1+2 = 3

```
  0001
+ 0010
------
  0011
```

Multiply 5*3 = 15



Most Common Operation in DSP

$A = B*C + D$

$E = F*G + A$

⋮

Multiply, Add, and Accumulate

MAC Instruction

MAC Operation

Typically 70 Clock Cycles With Ordinary Processors

Typically 1 Clock Cycle With Digital Signal Processors

Why Do We Need Digital Signal Processors?

Add and Subtract

Add and subtract operations are performed quite simply by general-purpose microprocessors in a single or very few clock cycles. Digital addition is similar to decimal add. Our example shows adding 1 plus 2. The result is the decimal 3.

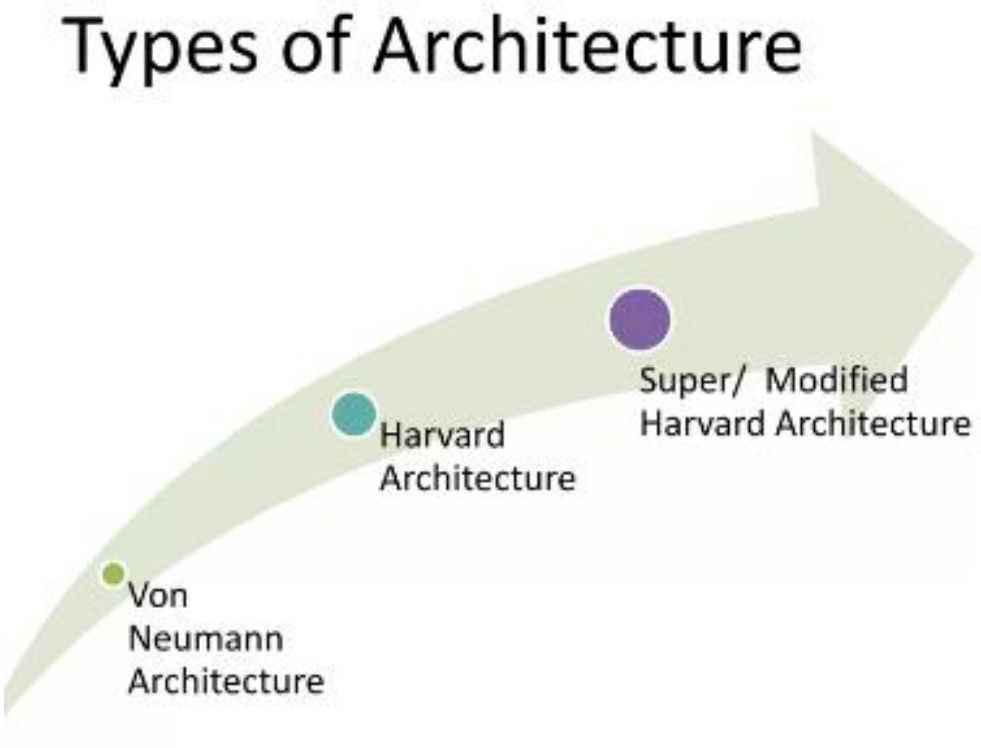
Multiply and Divide

The multiply and divide operations are more complex. A digital multiply operation consists of a series of *shift and add operations. example shows a multiplication of 3 & 5.* General-purpose microprocessors are quite slow in performing multiply and divide operations. They will typically sequentially execute a series of shift, add, and subtract operations from their microcode i.e.

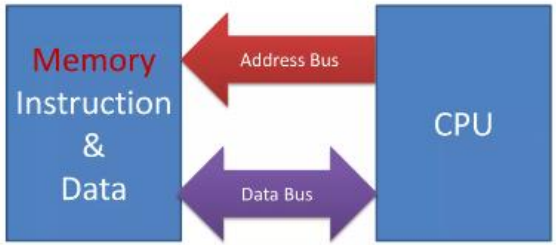
to perform a single multiply operation, it may consume many cycles to complete

The DSP performs multiplication in a single cycle by implementing all shift and add operations in parallel.

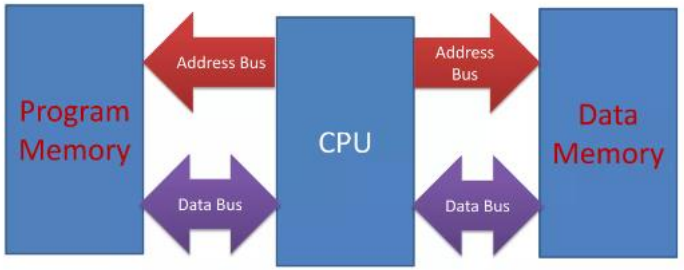
TYPES OF ARCHITECTURE



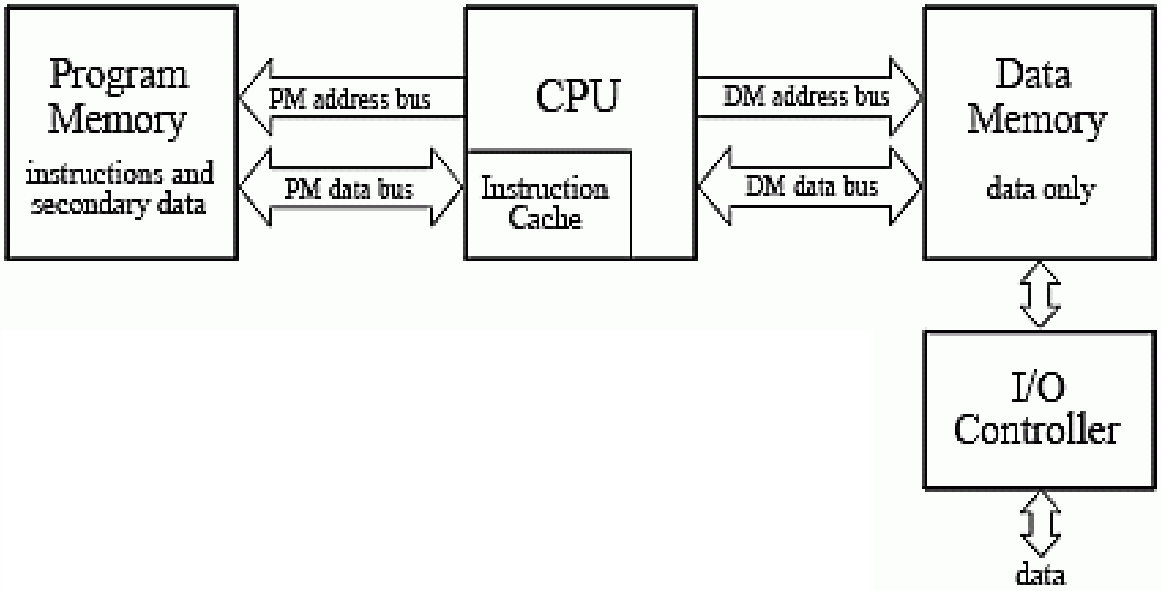
Von Neumann Architecture



Harvard Architecture



c. Super Harvard Architecture (*dual memory, instruction cache, I/O controller*)



Fixed vs. Floating Point

Characteristic	Floating point 32-bit	Fixed point 16-bit
Dynamic range	much larger	smaller
Resolution	comparable	comparable
Ease of programming	comparable	comparable
Compiler efficiency	much easier	more difficult
Power consumption	more efficient	less efficient
Chip cost	comparable	comparable
System cost	comparable	comparable
Design cost	less	more
Time to market	faster	slower


thank
you