SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

COURSE NAME :19IT301 COMPUTER ORGANIZATION AND ARCHITECTURE

II YEAR /III SEMESTER

Unit 5: I/O ORGANIZATION AND PARALLELISM

Topic 6: Standard I/O Interfaces (PCI, SCSI, USB)

Standard I/O interfaces

- I/O device is connected to a computer using an interface circuit.
- Do we have to design a different interface for every combination of an I/O device and a computer?
- A practical approach is to develop standard interfaces and protocols.
- A personal computer has:
  - A motherboard which houses the processor chip, main memory and some I/O interfaces.
  - A few connectors into which additional interfaces can be plugged.
- Processor bus is defined by the signals on the processor chip.
  - Devices which require high-speed connection to the processor are connected directly to this bus.

Standard I/O interfaces (contd..)

- Because of electrical reasons only a few devices can be connected directly to the processor bus.
- Motherboard usually provides another bus that can support more devices.
  - Processor bus and the other bus (called as expansion bus) are interconnected by a circuit called “bridge”.
  - Devices connected to the expansion bus experience a small delay in data transfers.
- Design of a processor bus is closely tied to the architecture of the processor.
  - No uniform standard can be defined.
- Expansion bus however can have uniform standard defined.

Standard I/O interfaces (contd..)

A number of standards have been developed for the expansion bus.

Some have evolved by default.

For example, IBM's Industry Standard Architecture.

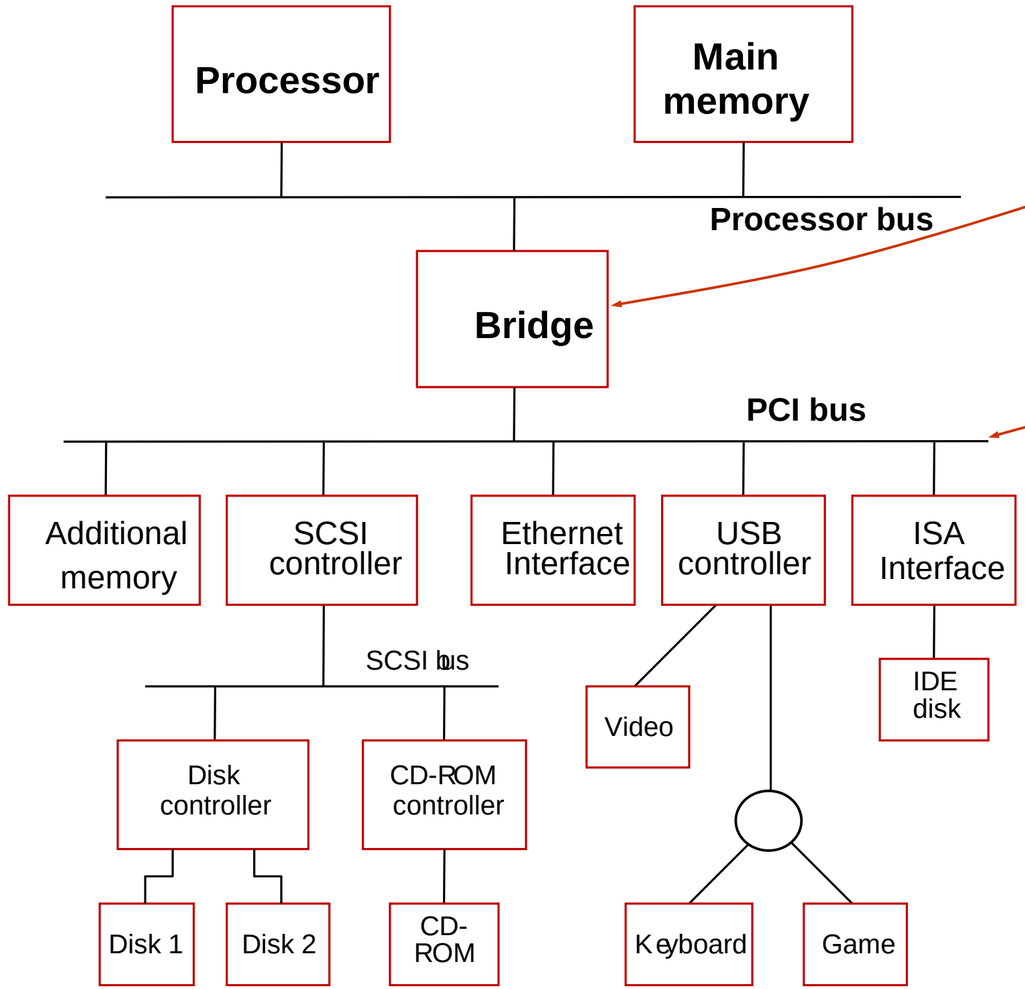
Three widely used bus standards:

PCI (Peripheral Component Interconnect)

SCSI (Small Computer System Interface)

USB (Universal Serial Bus)

Standard I/O interfaces (contd..)



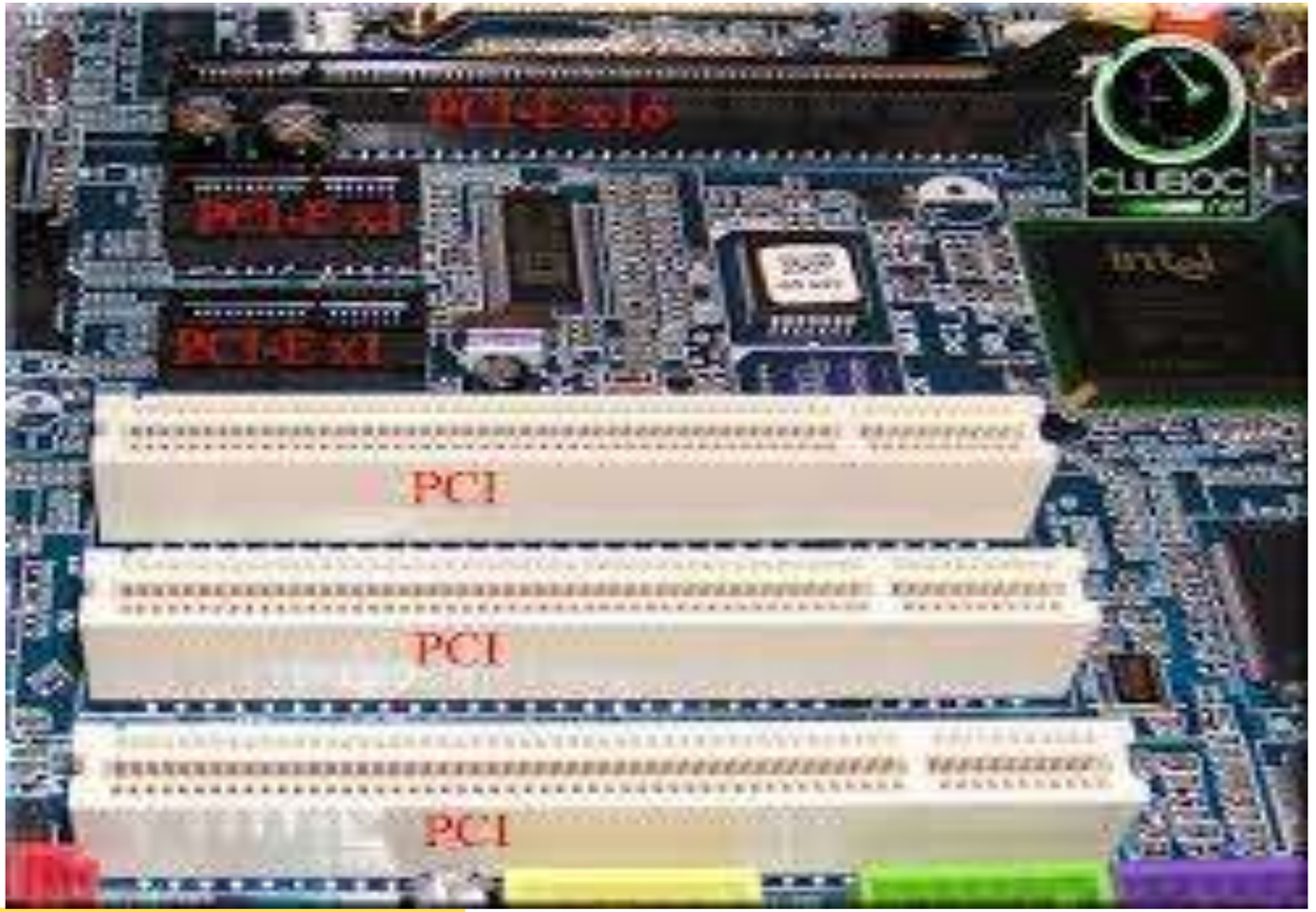
Bridge circuit translates signals and protocols from processor bus to PCI bus.

Expansion bus on the motherboard

PCI Bus

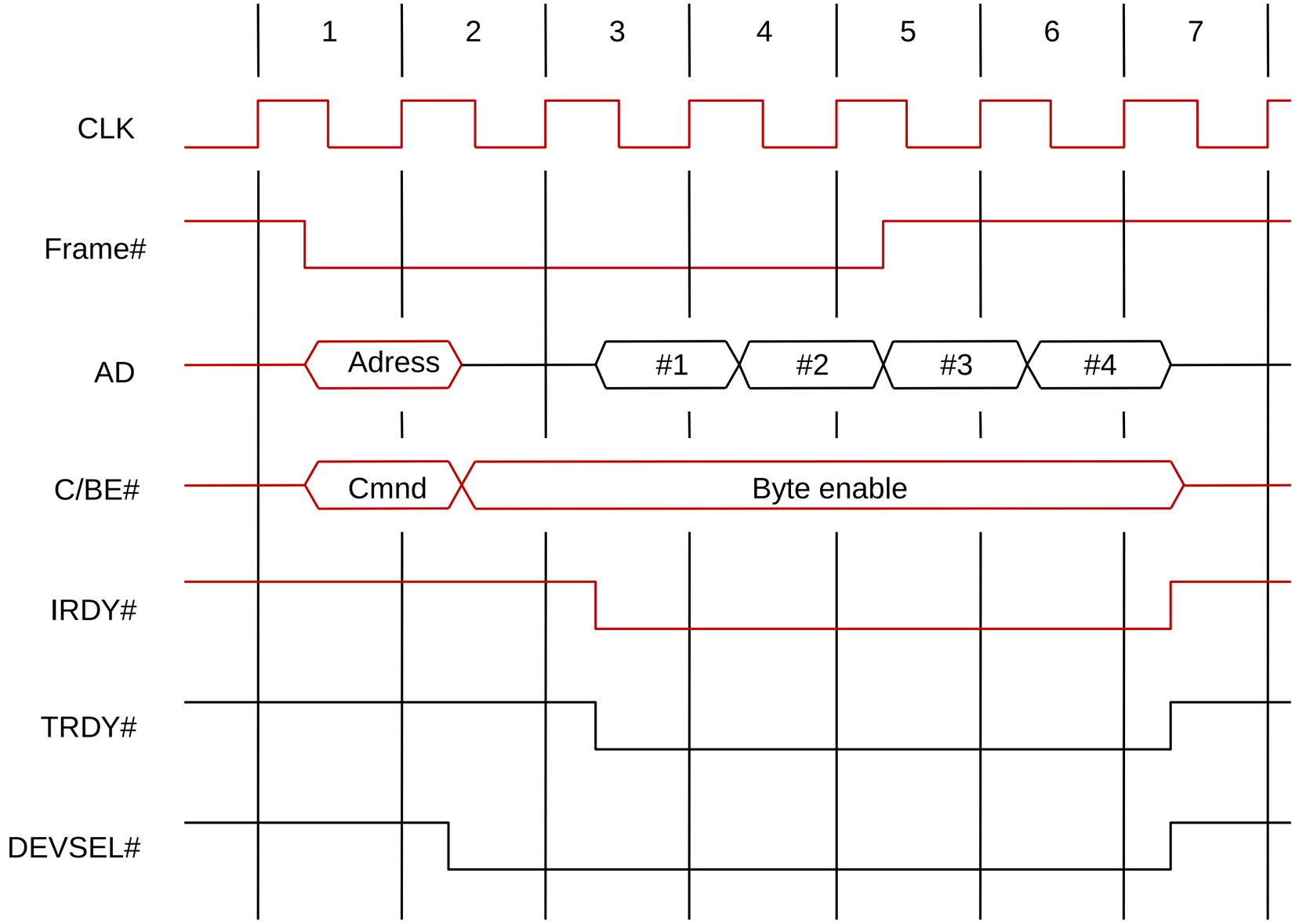
- *Peripheral Component Interconnect*
- Introduced in 1992
- Low-cost bus
- Processor independent
- Plug-and-play capability
- In today's computers, most memory transfers involve a burst of data rather than just one word. The PCI is designed primarily to support this mode of operation.
- The bus supports three independent address spaces: memory, I/O, and configuration.
- A master is called an initiator in PCI terminology. The addressed device that responds to read and write commands is called a target.


ET-PCI1610 V2


PCI
PCI
PCI

Data transfer signals on the PCI bus(62 0r 94 pins).

Name	Function
CLK	A 33-MHz or 66-MHz clock.
FRAME#	Sent by the initiator to indicate the duration of a transaction.
AD	32 address/data lines, which may be optionally increased to 64.
C/BE#	4 command/byte-enable lines (8 for a 64-bit bus).
IRD Y#, TRD Y#	Initiator-ready and Target-ready signals.
DEVSEL#	A response from the device indicating that it has recognized its address and is ready for a data transfer transaction.
IDSEL#	Initialization Device Select.



A read operation on the PCI bus

Device Configuration

- When an I/O device is connected to a computer, several actions are needed to configure both the device and the software that communicates with it.
- PCI incorporates in each I/O device interface a small configuration ROM memory that stores information about that device.
- The configuration ROMs of all devices are accessible in the configuration address space. The PCI initialization software reads these ROMs and determines whether the device is a printer, a keyboard, an Ethernet interface, or a disk controller. It can further learn bout various device options and characteristics.
- Devices are assigned addresses during the initialization process.
- This means that during the bus configuration operation, devices cannot be accessed based on their address, as they have not yet been assigned one.
- Hence, the configuration address space uses a different mechanism. Each device has an input signal called Initialization Device Select, IDSEL#
- Electrical characteristics:
  - PCI bus has been defined for operation with either a 5 or 3.3 V power supply

SCSI Bus

- The SCSI stands for Small Computer System Interface.
- It refers to a standard bus defined by the American National Standards Institute (ANSI) .
- In the original specifications of the standard, devices such as disks are connected to a computer via a 50-wire cable, which can be up to 25 meters in length and can transfer data at rates up to 5 megabytes/s.
- The SCSI bus standard has undergone many revisions, and its data transfer capability has increased very rapidly, almost doubling every two years.
- SCSI-2 and SCSI-3 have been defined, and each has several options.
- Because of various options SCSI connector may have 50, 68 or 80 pins.

SCSI Adapter Card

SCSI defined by ANSI (American national standards institute)
Narrow SCSI -8 bit data—8 devices
Wide SCSI –16 bit data—16 devices
Each signal 2 wires - 5v TTL—high voltage differential,3.3v low voltage differential
Maximum transfer rate 640 megabytes/s
DMA concept is used
Initiator- SCSI controller
Target– disk controller
Ability to overlap data transfer request----high speed
Disk controller –master
Disk drive-slave

The processor sends a command to the SCSI controller, which causes the following sequence of events:

1. **SCSI controller –initiator-requests for buses**
2. **If it wins the arbitration process, it selects the target controller and hands over control of the bus to it.**
3. Target starts output operation-initiator sends command specifying the required read operation.
4. Target understand the operataions and suspend and release the bus
5. **target performs disk seek operation- read data- request of bus- wins arbitration—restore suspended connection**
6. Data transfer from target to initiator-— suspend the bus again.
7. Command to next seek operation—continues step 5 and 6 until end of the data transfer
8. Data transfer terminated
9. Initiator stores data into the main memory using DMA
10. Scsi controller sends an interrupt to the processor to inform it that the requested operation has been completed.

Operation of SCSI bus from H/W point of view

Category	Name	Function
Data	– DB(0) to – DB(7)	Data lines: Carry one byte of information during the information transfer phase and identify device during arbitration, selection and reselection phases
	– DB(P)	Parity bit for the data bus
Phase	– BSY	Busy: Asserted when the bus is not free
	– SEL	Selection: Asserted during selection and reselection
Information type	– C/D	Control/Data: Asserted during transfer of control information (command, status or message)
	– MSG	Message: indicates that the information being transferred is a message

Table 4. The SCSI bus signals.

Table 4. The SCSI bus signals.(*cont*.)

Category	Name	Function
Handshake	– REQ	Request: Asserted by a target to request a data transfer cycle
	– ACK	Acknowledge: Asserted by the initiator when it has completed a data transfer operation
Direction of transfer	– I/O	Input/Output: Asserted to indicate an input operation (relative to the initiator)
Other	– ATN	Attention: Asserted by an initiator when it wishes to send a message to a target
	– RST	Reset: Causes all device controls to disconnect from the bus and assume their start-up state

Main Phases involved

- Arbitration
  - A controller requests the bus by asserting BSY and by asserting it’s associated data line
  - When BSY becomes active, all controllers that are requesting bus examine data lines
- Selection
  - Controller that won arbitration selects target by asserting SEL and data line of target. After that initiator releases BSY line.
  - Target responds by asserting BSY line
  - Target controller will have control on the bus from then
- Information Transfer
  - Handshaking signals are used between initiator and target
  - At the end target releases BSY line
- Reselection

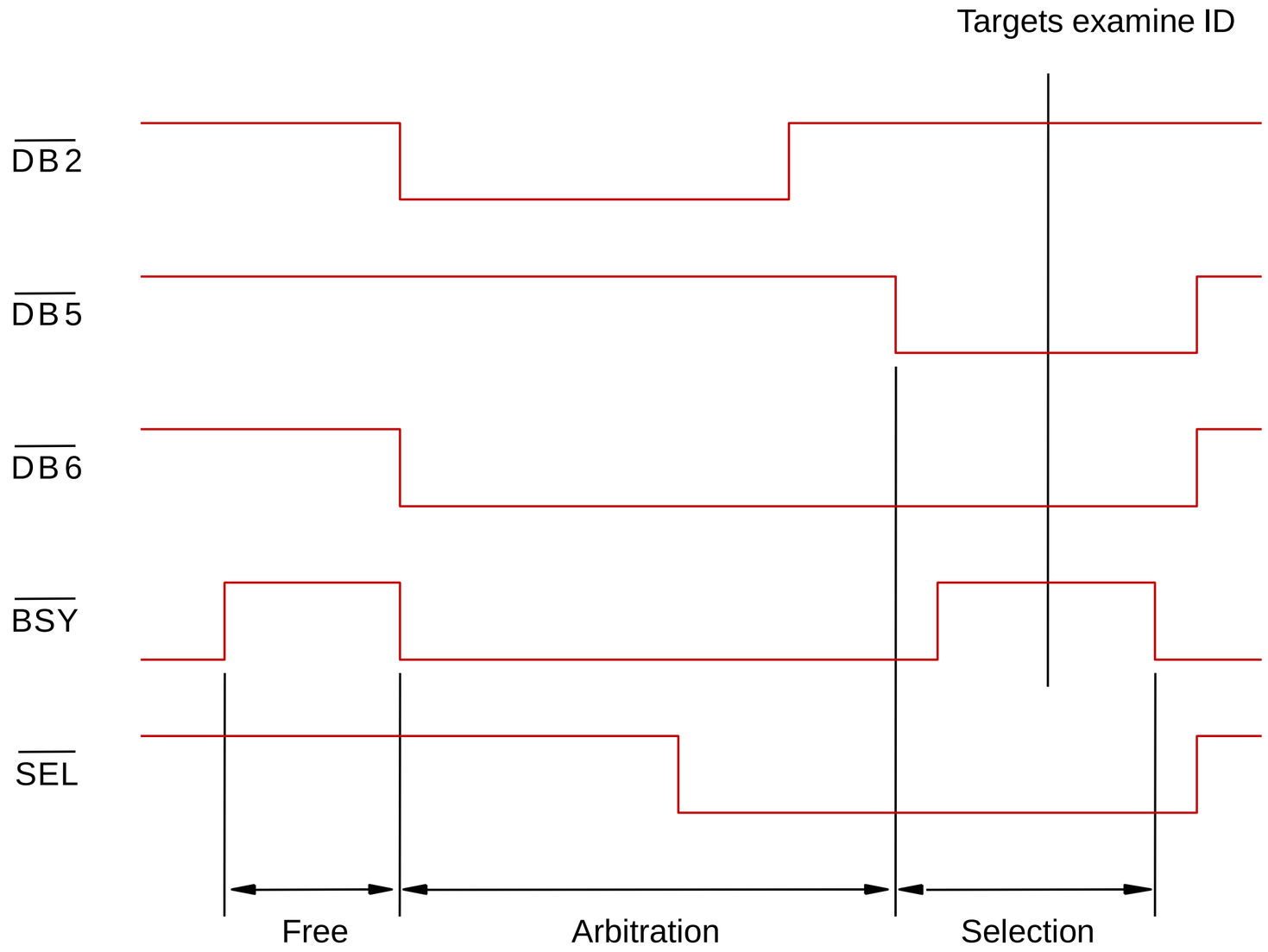


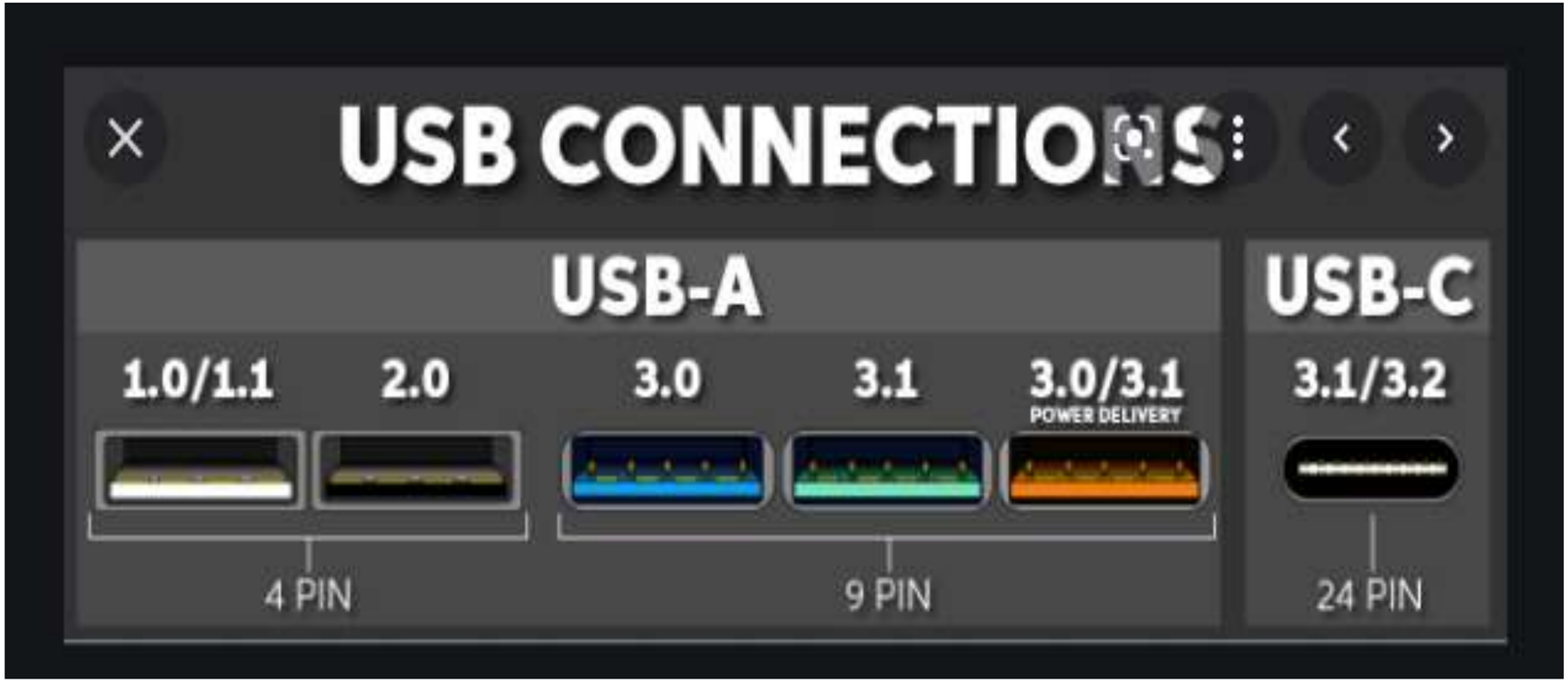
Figure 42. Arbitration and selection on the SCSI bus.
Device 6 wins arbitration and selects device 2.

USB

- Universal Serial Bus
  - Originally developed in 1995 by a consortium including
    - Compaq, HP, Intel, Lucent, Microsoft, and Philips
    - Serial data transfer

Key objectives:

- Simple low- cost mechanism to connect devices to the computer.
- Wide range of data transfer characteristics for I/O devices including telephone and internet connection.
- User convenience through plug and play


USB CONNECTIONS
USB-A
USB-C
1.0/1.1
2.0
3.0
3.1
3.0/3.1
POWER DELIVERY
3.1/3.2
4 PIN
9 PIN
24 PIN


USB TYPE A
USB TYPE B
USB 3.0
USB MINI
USB MICRO
USB TYPE C
USB MICRO B

Applications

1.USB Type-A
•TV
•Computers
•Keyboards
•Flash drives
•Gaming consoles

2.USB Type-B
•Printers
•Scanners

3.Mini-USB
•Digital camera
•MP3 players
4.Micro-USB
•Android phones
•Android tablets
•Digital cameras
5.USB Type-C
Today, almost all smartphones, microphones, and laptops
Besides, it supports USB Power Delivery of up to 100 Watt, making it a perfect companion for fast charging and data transfer of power-hungry devices like laptops.
Where commonly found?
•Laptops
•Charging station

Type A, B or C usually **refers to the physical design of the plugs and the ports**, while the versions determine the functionality and the speed of the USB cable.

USB speed

USB 1.0	Low-Speed	1.5Mbps
USB 1.1	Full-Speed	12Mbps
USB 2.0	Hi-Speed	480Mbps
USB 3.0	SuperSpeed	5Gbps
USB 3.1 Gen 1	SuperSpeed	5Gbps
USB 3.1 Gen 2	SuperSpeed+	10Gbps
USB 3.2 Gen 1	SuperSpeed USB	5Gbps
USB 3.2 Gen 2	SuperSpeed USB 10Gbps	10Gbps
USB 3.2 Gen 2×2	SuperSpeed USB 20Gbps	20Gbps
USB4 20Gbps	USB20Gbps	20Gbps
USB4 40Gbps	USB40Gbps	40Gbps

Features

1. Asynchronous serial communication.
2. Attachment is detected and device is configured automatically.
1. Single standard connector.
2. 127 devices can be connected via hubs.
3. Three device speeds:
4. Low
5. Full
6. High
7. Power: 5V, 100mA-500mA
8. Error detection/recovery is automatic.

USB is a master/slave protocol

4 types of data transfer:

–Control

–Bulk

volume, non-time-critical data

–Interrupt

polled, low-volume data

–Isochronous

volume, time-critical data

USB (cont'd)

USB architecture

- –To meet the requirements like low cost flexibility, and high BW
- –Tree structure ,to add or remove devices easily
- –USB host controller
  - Initiates transactions over USB
- –Hub
- Copy the message of root and broadcast to devices. Addressed device will respond to that message.
- –Root hub
  - Provides connection points

USB architecture (cont'd)

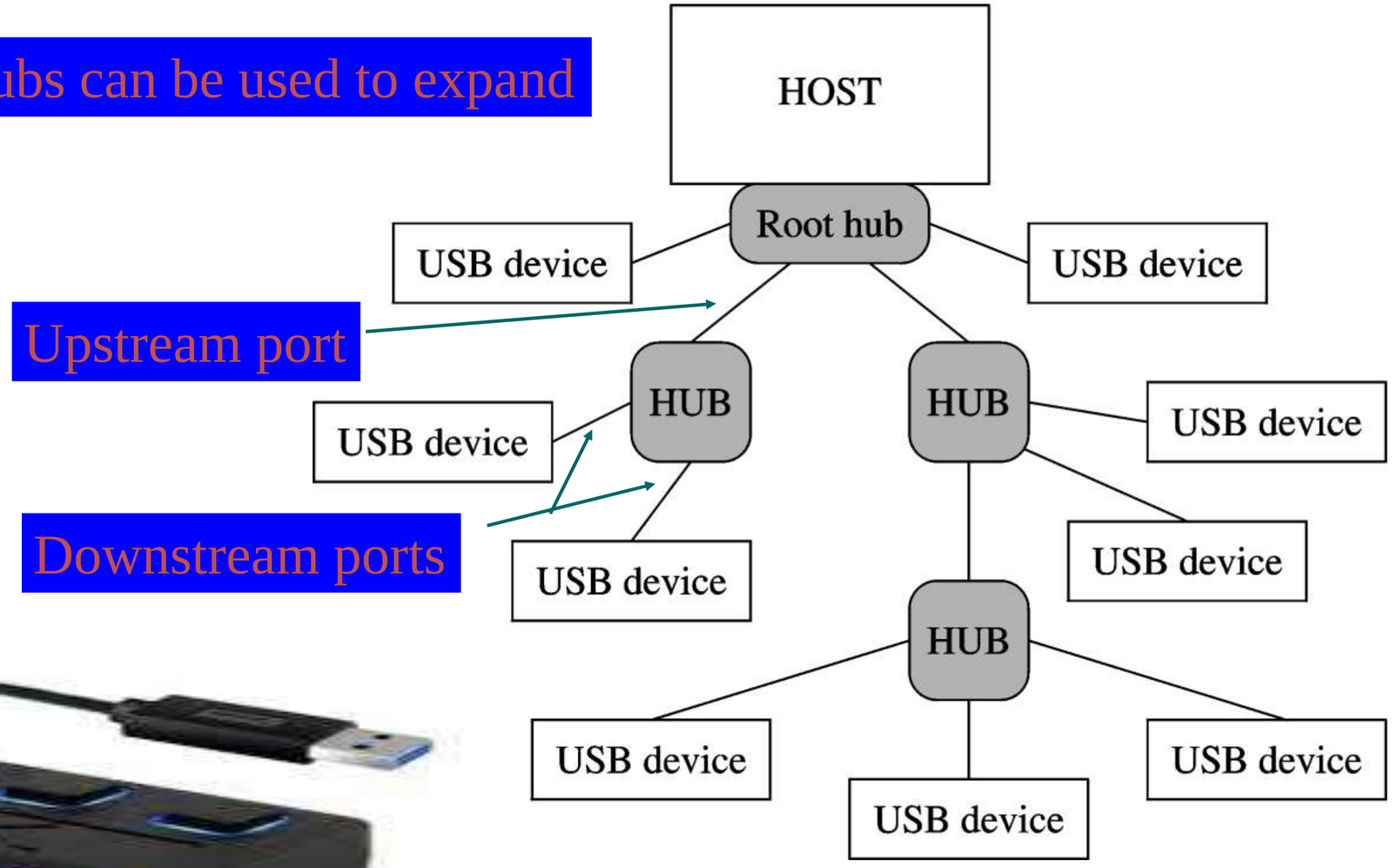
Each I/O device is connected through a serial point-to-point connection

Polling: a device may send a message only in response to a poll message from the host. i.e no two devices can send messages at the same time.

Split bus operation: special commands to A as shown in fig. Start and end the split traffic mode of operation.

USB tree structure

Hubs can be used to expand



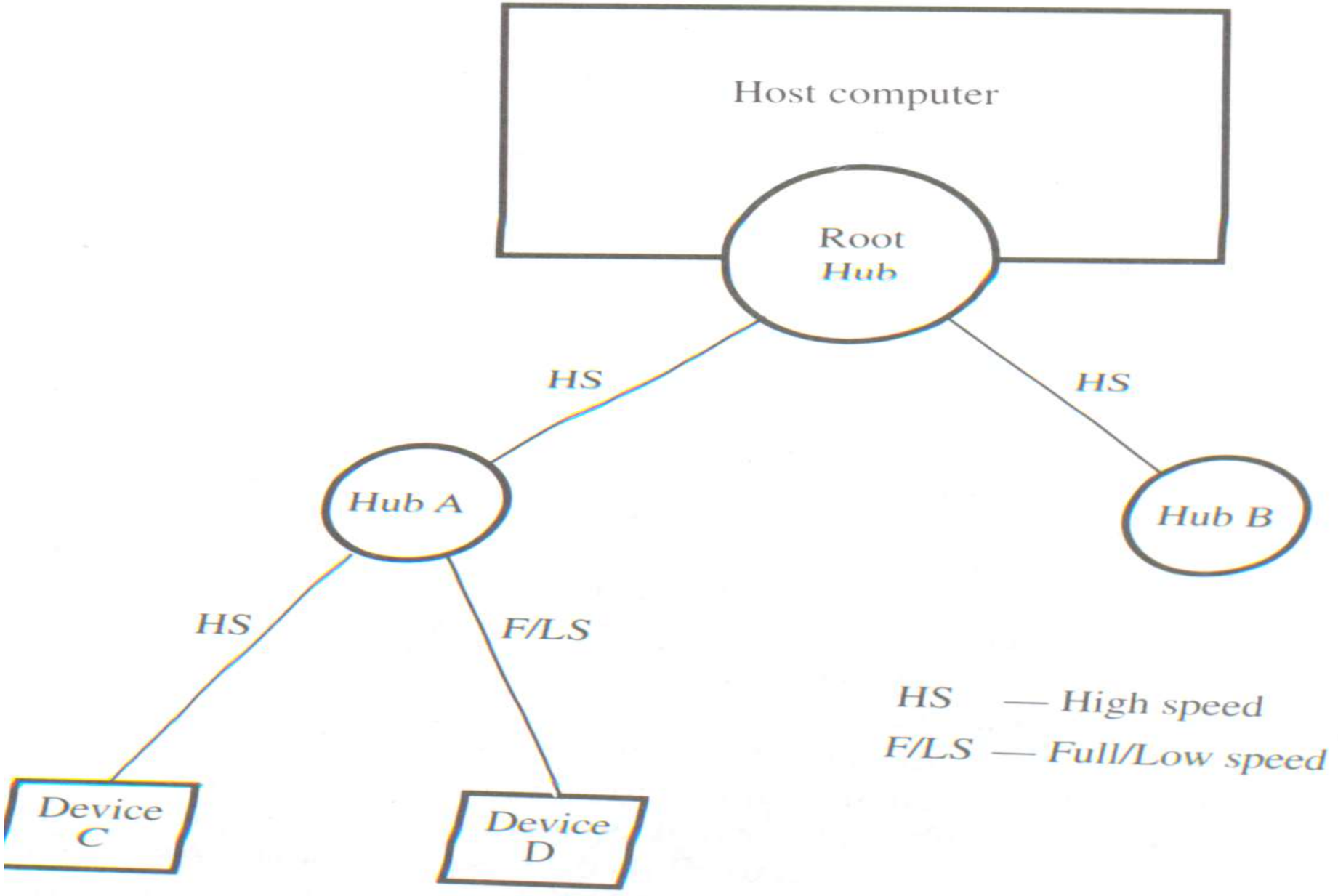


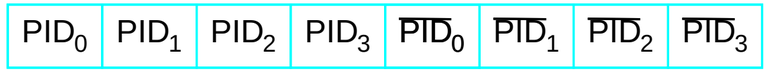
Figure 4.44 Split bus operation.

Addressing

- Root hub attached to a host as a single device
- Host software communicates with individual devices.
- Addresses are assigned arbitrarily. When a device is first connected to a hub or when it is powered on– address is 0.
- It Records this as status information and sends reset signal and collect details about the device.
- For power off similar procedure and tables are updated.
- If a hub is disconnected—all devices connected to this hub are disconnected.

USB protocols:

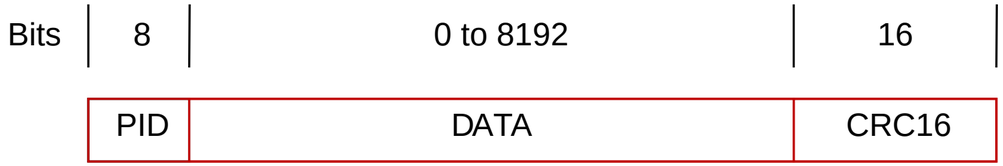
- control packet– addressing initiate device, ACK of data & indication of error.
- Data pocket– carries information
- Control pockets used for controlling data transfer operations are called token packets.
- Locations in the device such as status ,control and data registers are called endpoints (ENDP).
- End points are identified by 4 bit number i.e device may have 16 input /output pairs of endpoints. CRC based on address and ENDP.



(a) Packet identifier field

(b) Token packet, IN or OUT

Control packets used for controlling data transfer operations are called token packets.



(c) Data packet

Figure 45. USB packet format.

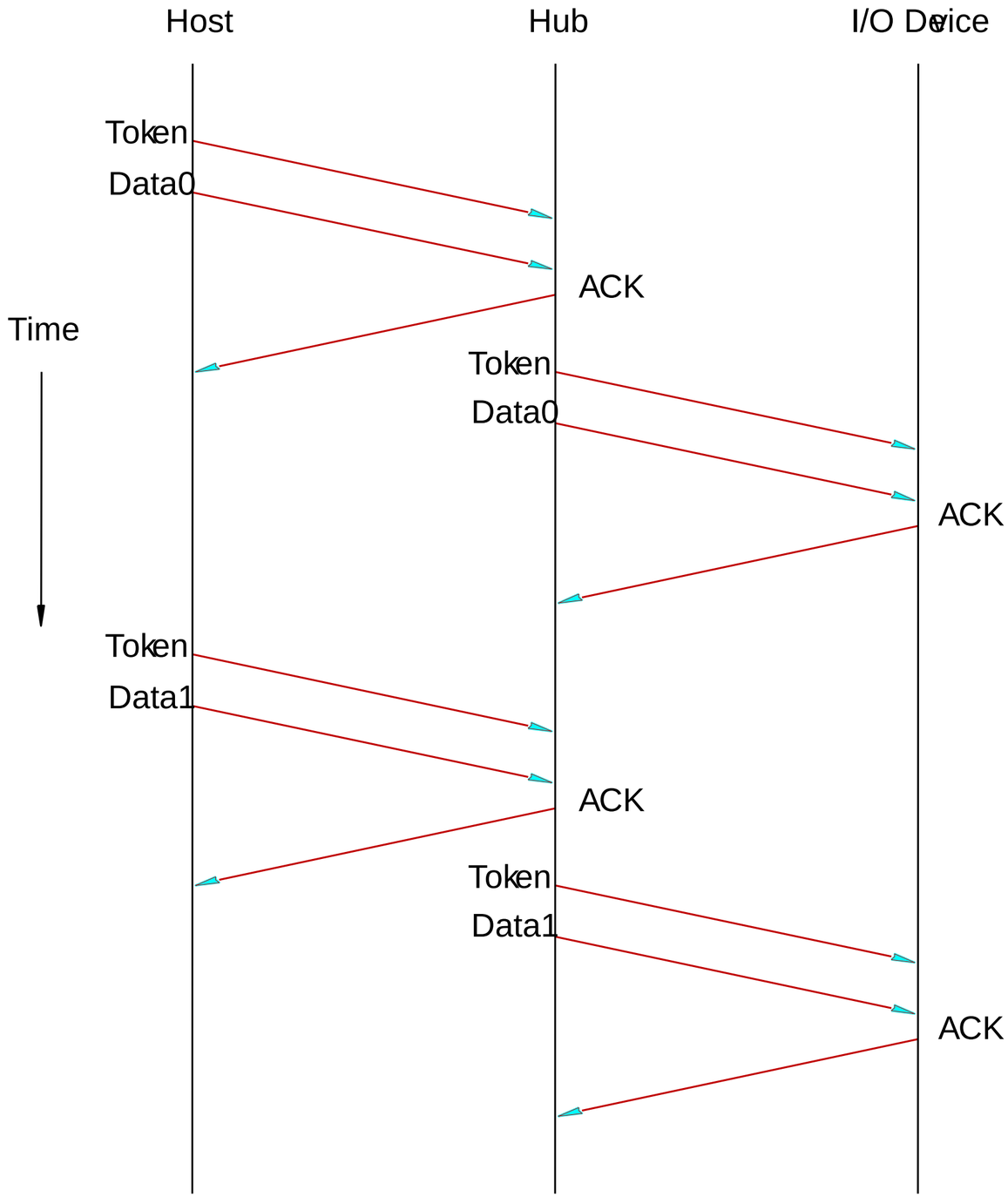


Figure: An output transfer

USB (cont'd)

- USB transactions
  - Transfers are done in one or more transactions
    - Each transaction consists of several packets
  - Transactions may have between 1 and 3 phases
    - Token packet phase
      - Specifies transaction type and target device address
    - Data packet phase (optional)
      - Maximum of 1023 bytes are transferred
    - Handshake packet phase
      - Provides feedback on whether data has been received without error

Isochronous traffic on USB:

Isochronous means successive events are separated by equal period of times.

i.e continuous stream of digitized samples that arrive at regular intervals, synchronized with the sampling clock.

Key objective: To support the transfer of isochronous data such as sampled voice in a simple manner.

To provide time reference to sampling process transmission over USB is divided into frames of equal length(1 ms).

11 bit frame number –to provide longer periods.

USB (cont'd)

- advantages of USB
  - –Power distribution
    - Simple devices can be bus-powered
      - –Examples: mouse, keyboards, floppy disk drives, wireless LANs, …
  - –Control peripherals
    - Possible because USB allows data to flow in both directions
  - –Expandable through hubs
  - –Power conservation
    - Enters suspend state if there is no activity for 3 ms
  - –Error detection and recovery
    - Uses CRC

Electrical Characteristics

- The cables used for USB connections consist of four wires.
- Two are used to carry power, +5V and Ground.
  - Thus, a hub or an I/O device may be powered directly from the bus, or it may have its own external power connection.
- The other two wires are used to carry data.
- Different signaling schemes are used for different speeds of transmission.
  - At low speed, 1s and 0s are transmitted by sending a high voltage state (5V) on one or the other o the two signal wires. For high-speed links, differential transmission is used.

Assessment

What is STD Interface circuit?
What is PCI interface?
What is SCSI interface?
What is USB interface?

Reference

1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, “Computer Organization”, McGraw-Hill, 6th Edition 2012.