SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

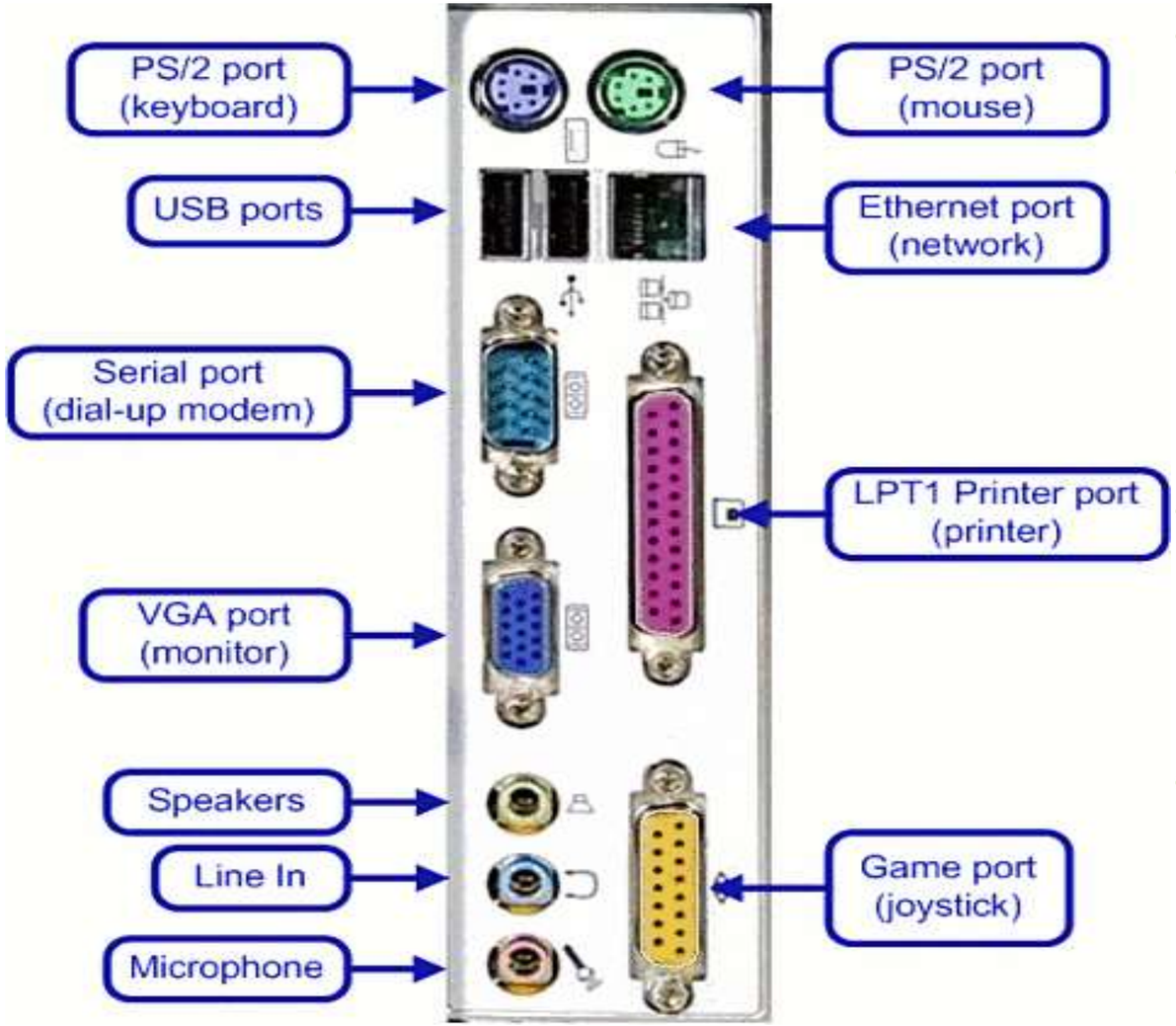
COURSE NAME :19IT301 COMPUTER ORGANIZATION AND ARCHITECTURE

II YEAR /III SEMESTER

Unit 5: I/O ORGANIZATION AND PARALLELISM

Topic 5: Interface circuits

Interface circuits

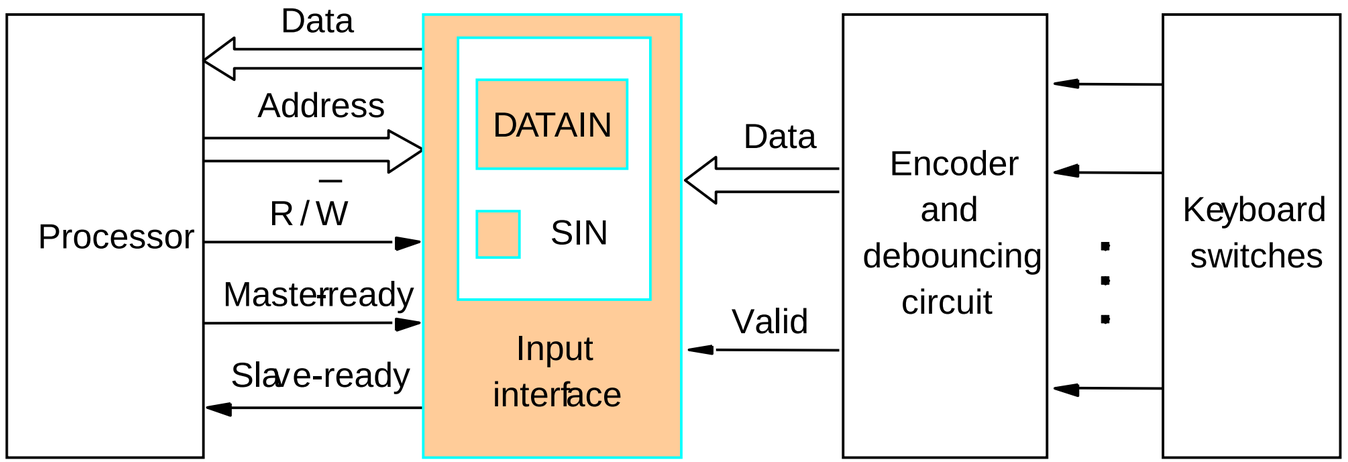


- I/O interface consists of the circuitry required to connect an I/O device to a computer bus.
- Interface which connects to the computer has bus signals for:
  - Address,
  - Data
  - Control
- Interface which connects to the I/O device has:
  - Datapath and associated controls to transfer data between the interface and the I/O device.
  - This side is called as a "port".
- Ports can be classified into two:
  - Parallel port,
  - Serial port.

Interface circuits (contd..)

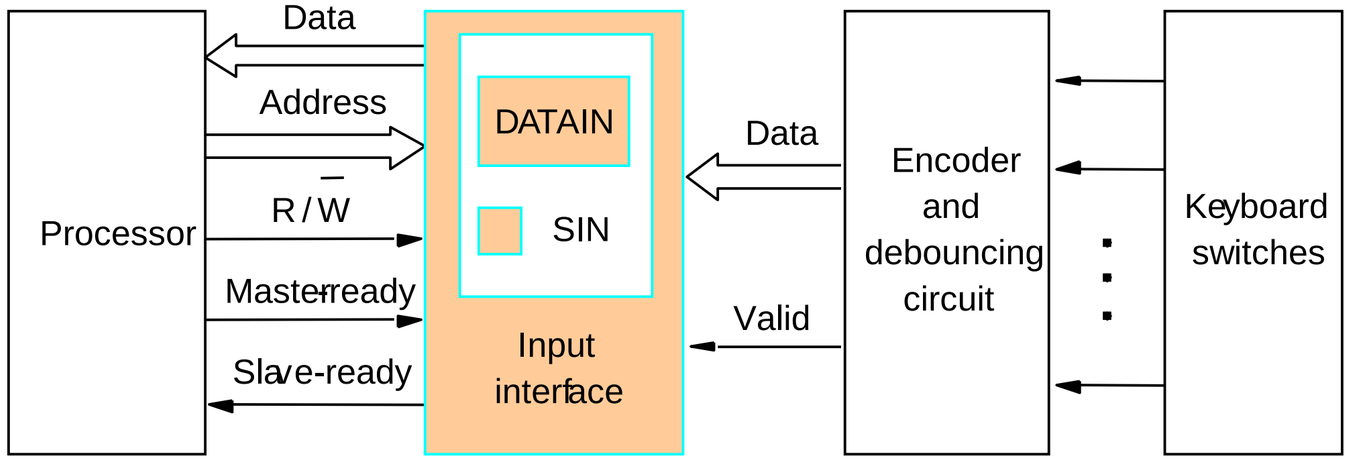
- Parallel port transfers data in the form of a number of bits, normally 8 or 16 to or from the device.
- Serial port transfers and receives data one bit at a time.
- Processor communicates with the bus in the same way, whether it is a parallel port or a serial port.
  - Conversion from the parallel to serial and vice versa takes place inside the interface circuit.

Parallel port



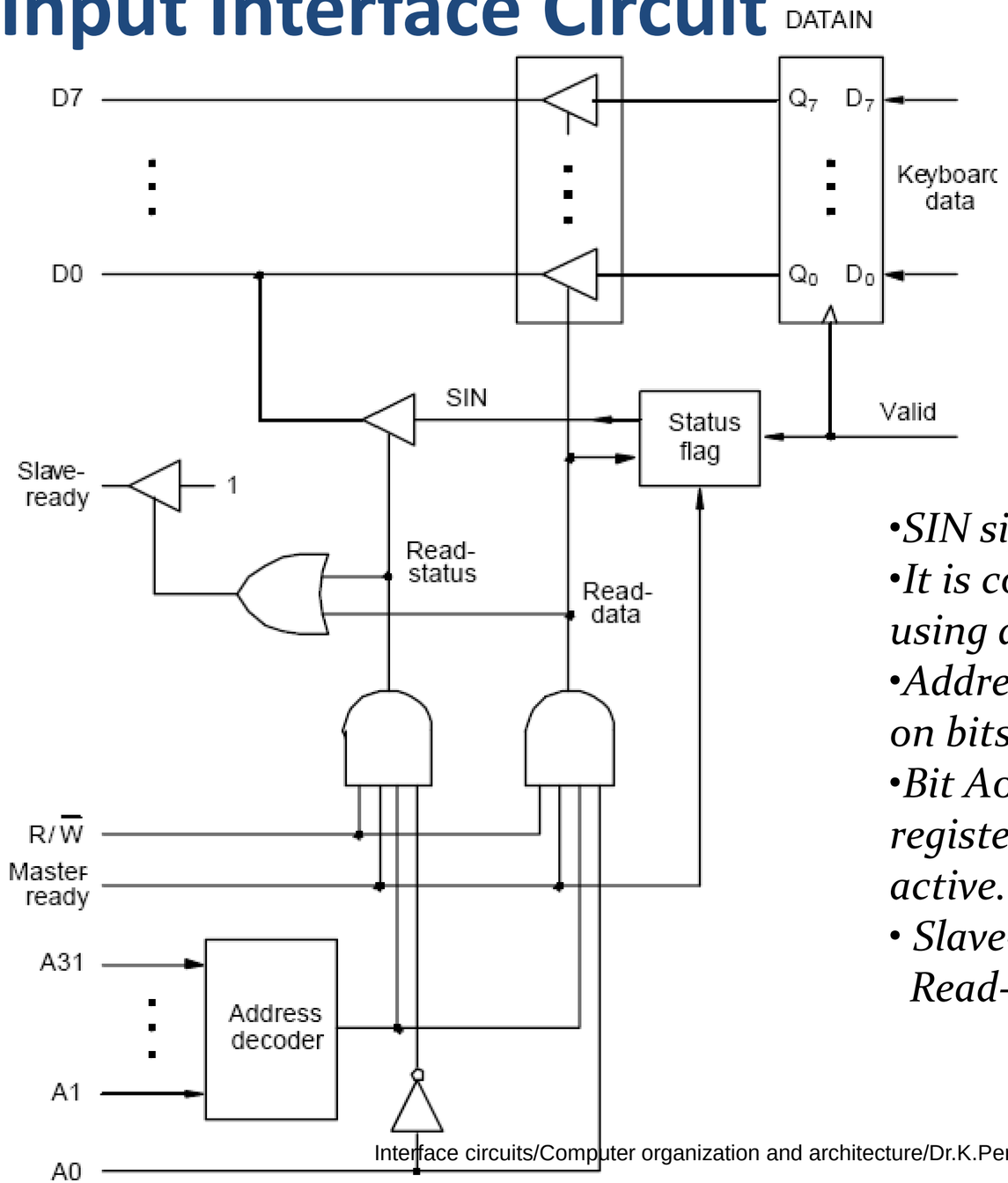
- *Keyboard is connected to a processor using a parallel port.*
- *Processor is 32-bits and uses memory-mapped I/O and the asynchronous bus protocol.*
- *On the processor side of the interface we have:*
  - *Data lines.*
  - *Address lines*
  - *Control or R/W line.*
  - *Master-ready signal and*
  - *Slave-ready signal.*

Parallel port (contd..)



- *On the keyboard side of the interface:*
  - *Encoder circuit which generates a code for the key pressed.*
  - *Debouncing circuit which eliminates the effect of a key bounce (a single key stroke may appear as multiple events to a processor).*
  - *Data lines contain the code for the key.*
  - *Valid line changes from 0 to 1 when the key is pressed. This causes the code to be loaded into DATAIN and SIN to be set to 1.*

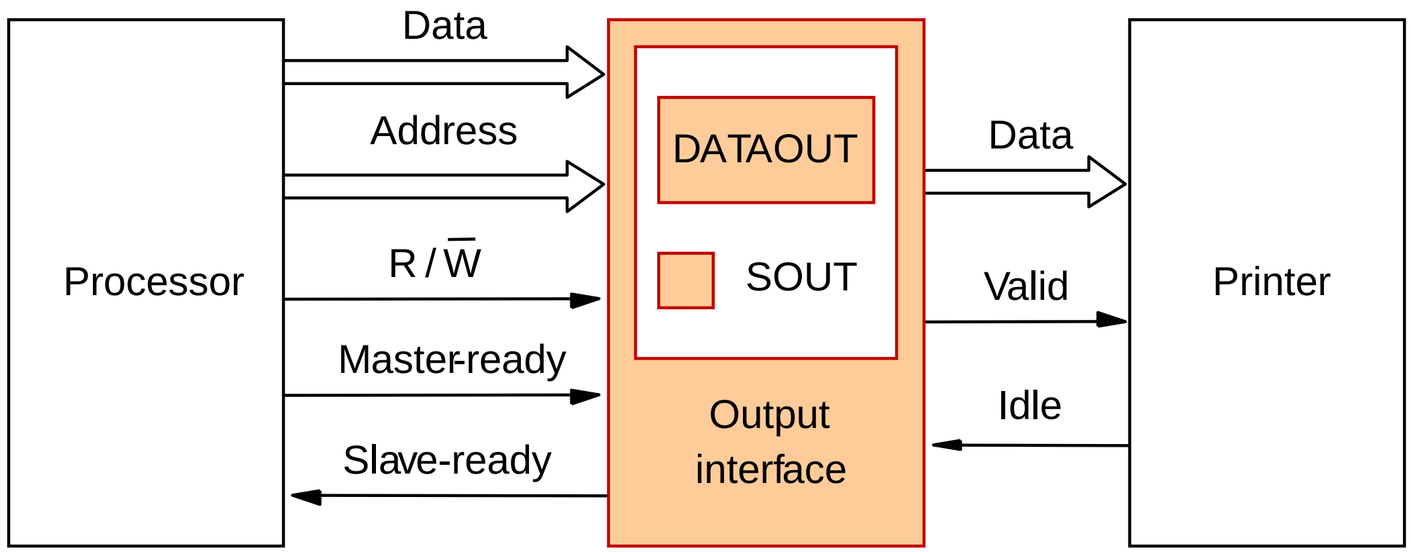
Input Interface Circuit



- *Output lines of DATAIN are are connected to the data lines of the bus by means of 3 state drivers*
- *Drivers are turned on when the processor issues a read signal and the address selects this register.*

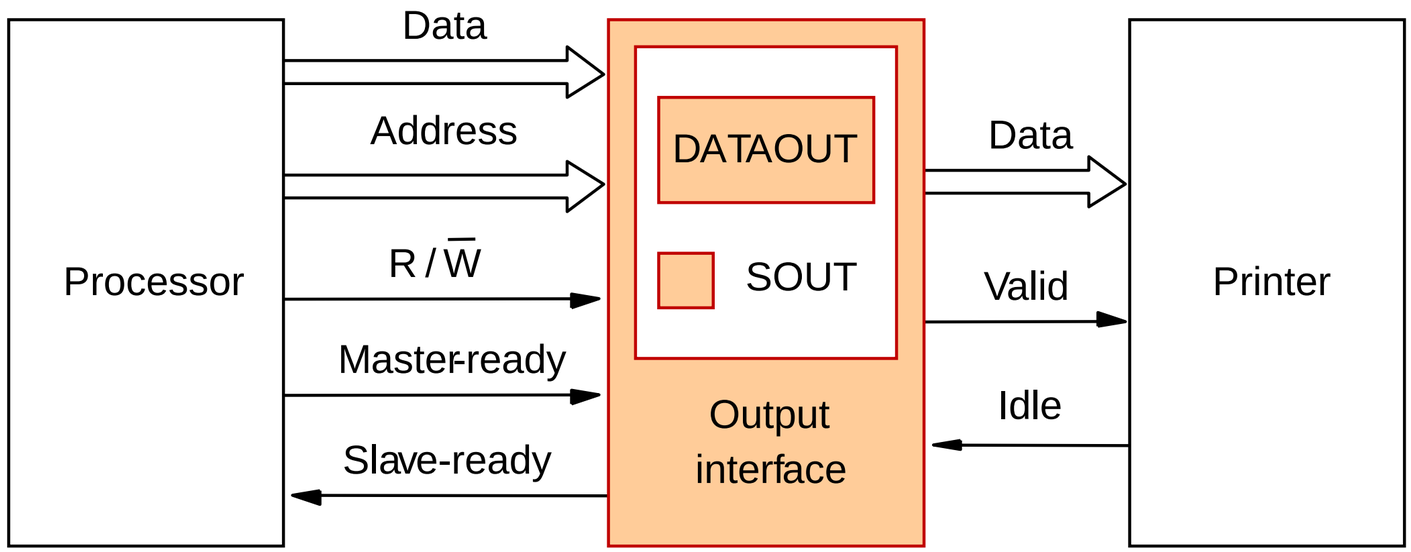
- *SIN signal is generated using a status flag circuit.*
- *It is connected to line D_0 of the processor bus using a three-state driver.*
- *Address decoder selects the input interface based on bits A_1 through A_{31}.*
- *Bit Ao determines whether the status or data register is to be read, when Master-ready is active.*
- *Slave-ready signal, when either the Read-status or Read-data is equal to 1, which depends on line A_0.*

Parallel port (contd..)



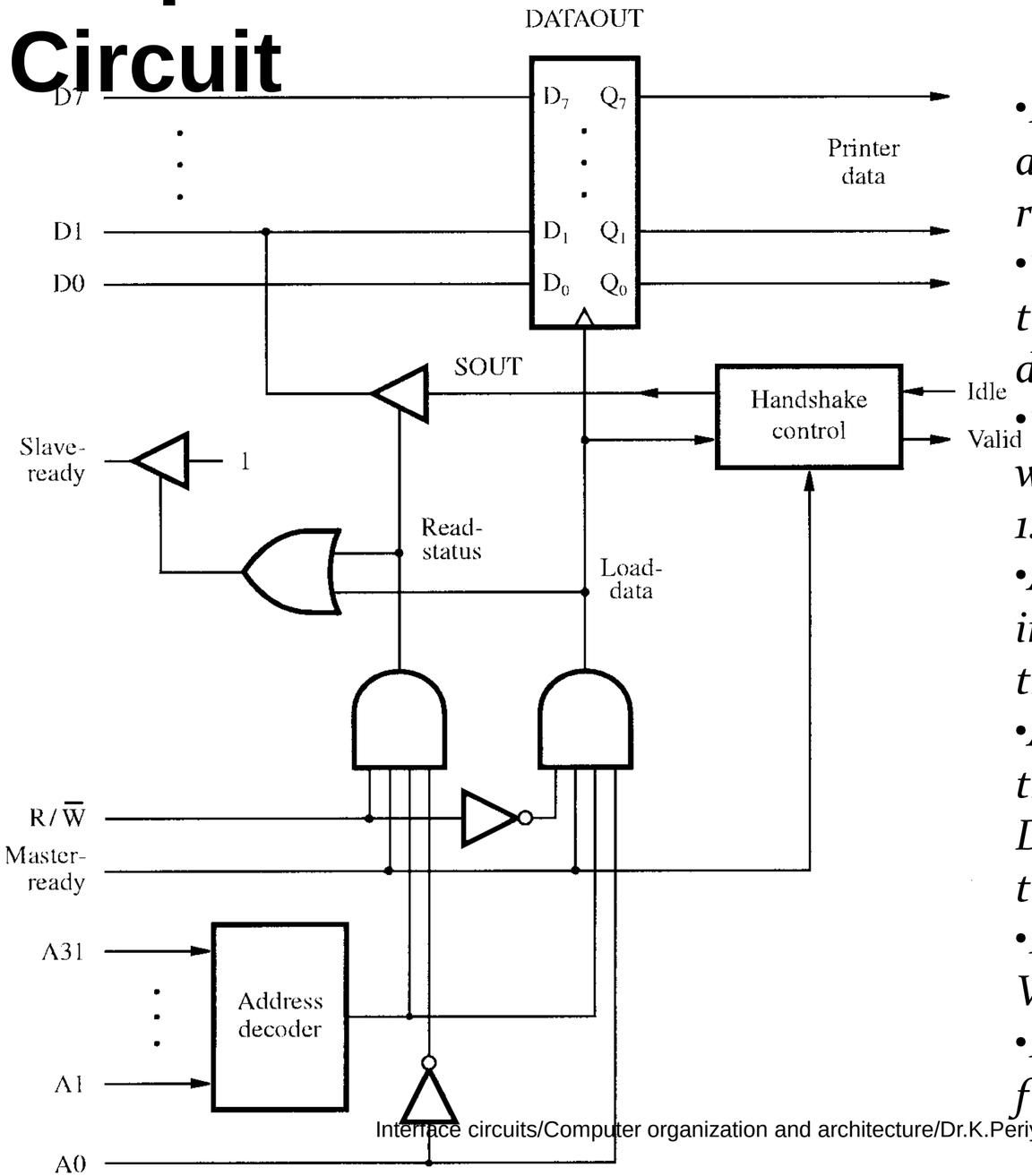
- *Printer is connected to a processor using a parallel port.*
- *Processor is 32 bits, uses memory-mapped I/O and asynchronous bus protocol.*
- *On the processor side:*
  - *Data lines.*
  - *Address lines*
  - *Control or R/W line.*
  - *Master-ready signal and*
  - *Slave-ready signal.*

Parallel port (contd..)

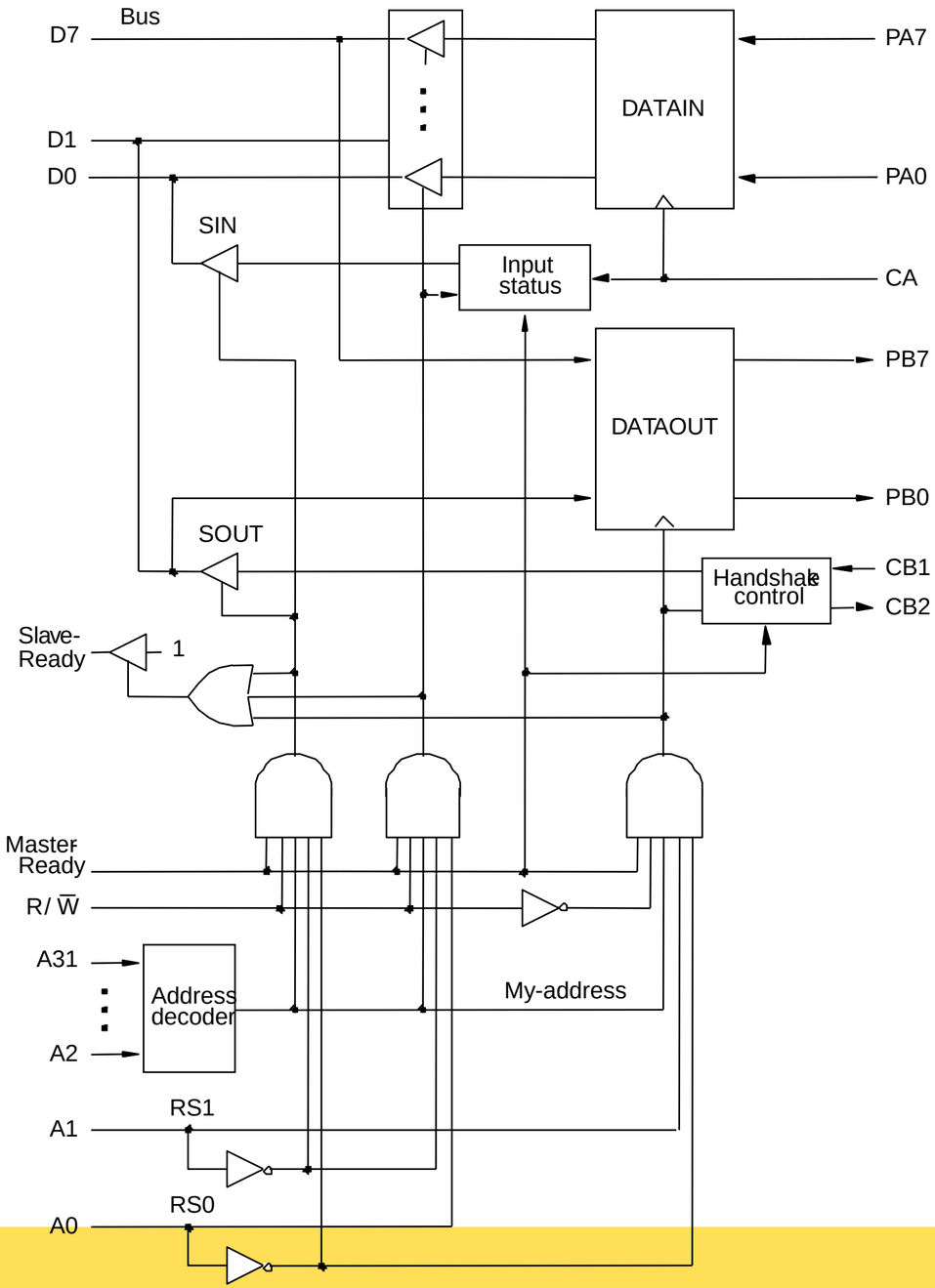


- *On the printer side:*
  - *Idle signal line which the printer asserts when it is ready to accept a character. This causes the SOUT flag to be set to 1.*
  - *Processor places a new character into a DATAOUT register.*
  - *Valid signal, asserted by the interface circuit when it places a new character on the data lines.*

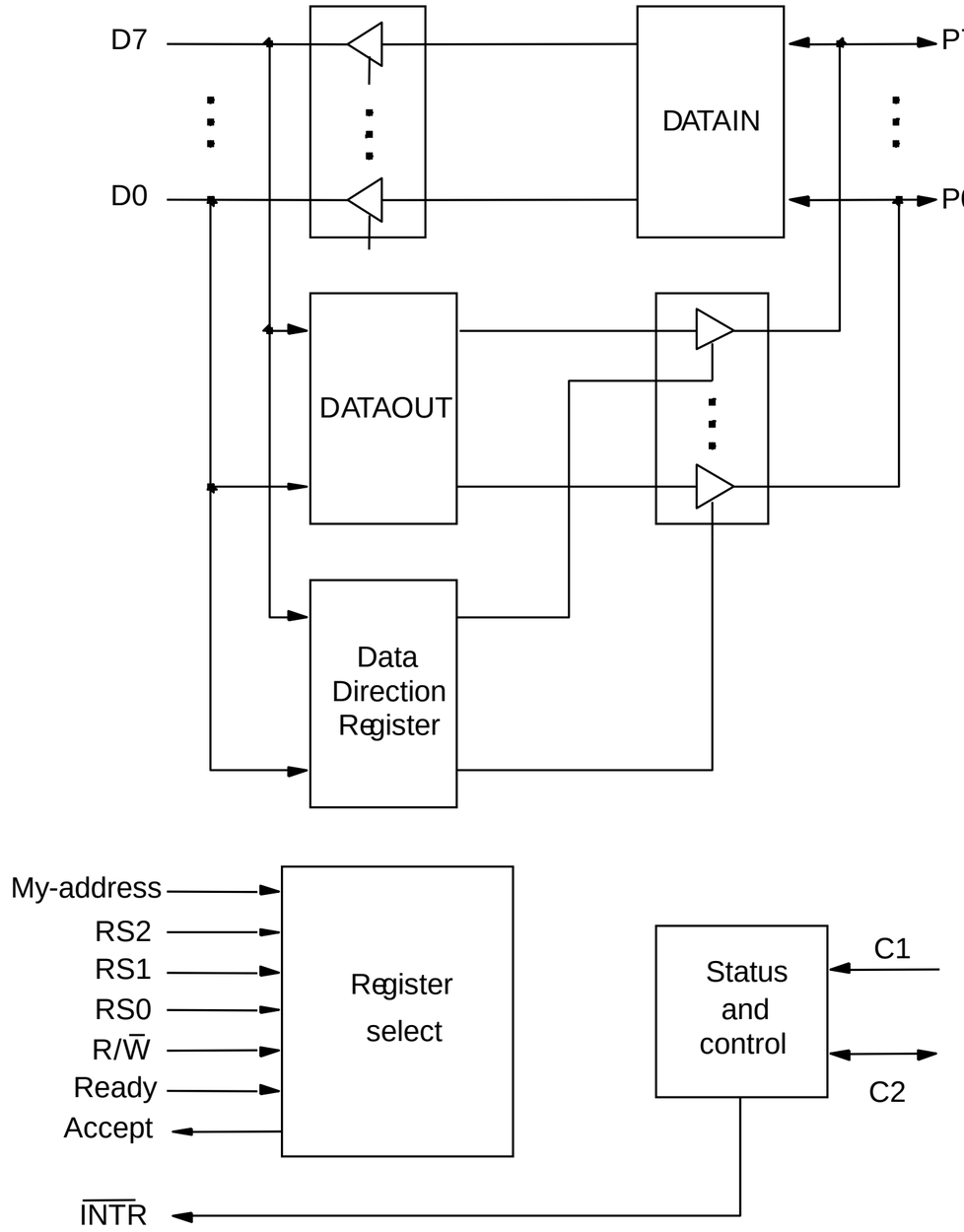
Output Interface Circuit



- *Data lines of the processor bus are connected to the DATAOUT register of the interface.*
- *The status flag SOUT is connected to the data line D1 using a three-state driver.*
- *The three-state driver is turned on, when the control Read-status line is 1.*
- *Address decoder selects the output interface using address lines A1 through A31.*
- *Address line A0 determines whether the data is to be loaded into the DATAOUT register or status flag is to be read.*
- *If the Load-data line is 1, then the Valid line is set to 1.*
- *If the Idle line is 1, then the status flag SOUT is set to 1.*



- *Combined I/O interface circuit.*
- *Address bits A2 through A31, that is 30 bits are used to select the overall interface.*
- *Address bits A1 through A0, that is, 2 bits select one of the three registers, namely, DATAIN, DATAOUT, and the status register.*
- *Status register contains the flags SIN and SOUT in bits 0 and 1.*
- *Data lines PA0 through PA7 connect the input device to the DATAIN register.*
- *DATAOUT register connects the data lines on the processor bus to lines PB0 through PB7 which connect to the output device.*
- *Separate input and output data lines for connection to an I/O device.*

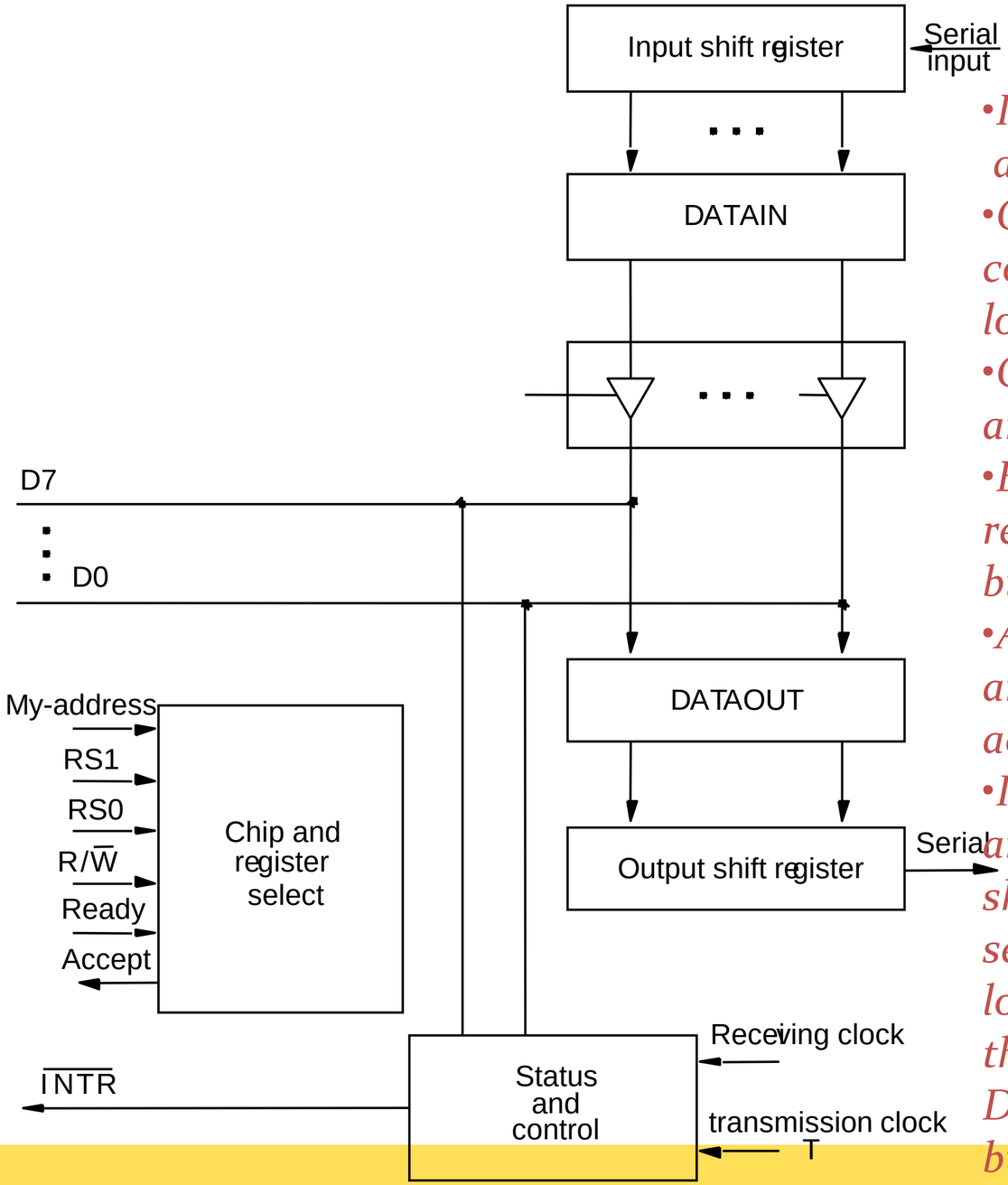


- *Data lines to I/O device are bidirectional.*
- *Data lines P7 through Po can be used for both input, and output.*
- *In fact, some lines can be used for input & some for output depending on the pattern in the Data Direction Register (DDR).*
- *Processor places an 8-bit pattern into a DDR.*
- *If a given bit position in the DDR is 1, the corresponding data line acts as an output line, otherwise it acts as an input line.*
- *C1 and C2 control the interaction between the interface circuit and the I/O devices.*
- *Ready and Accept lines are the handshake control lines on the processor bus side, and are connected to Master-ready & Slave-ready.*
- *Input signal My-address is connected to the output of an address decoder.*
- *Three register select lines that allow up to 8 registers to be selected.*

Serial port

- Serial port is used to connect the processor to I/O devices that require transmission of data one bit at a time.
- Serial port communicates in a bit-serial fashion on the device side and bit parallel fashion on the bus side.

  Transformation between the parallel and serial formats is achieved with shift registers that have parallel access capability.



- *Input shift register accepts input one bit at a time from the I/O device.*
- *Once all the 8 bits are received, the contents of the input shift register are loaded in parallel into DATAIN register.*
- *Output data in the DATAOUT register are loaded into the output shift register.*
- *Bits are shifted out of the output shift register and sent out to the I/O device one bit at a time.*
- *As soon as data from the input shift reg. are loaded into DATAIN, it can start accepting another 8 bits of data.*
- *Input shift register and DATAIN registers are both used at input so that the input shift register can start receiving another set of 8 bits from the input device after loading the contents to DATAIN, before the processor reads the contents of DATAIN. This is called as double-buffering.*

Serial port (contd..)

- Serial interfaces require fewer wires, and hence serial transmission is convenient for connecting devices that are physically distant from the computer.
- Speed of transmission of the data over a serial interface is known as the “bit rate”.
  - Bit rate depends on the nature of the devices connected.
- In order to accommodate devices with a range of speeds, a serial interface must be able to use a range of clock speeds.
- Several standard serial interfaces have been developed:
  - Universal Asynchronous Receiver Transmitter (UART) for low-speed serial devices.
  - RS-232-C for connection to communication links.

Assessment

What is Interface circuit?
What is Serial interface?
What is parallel interface?
What is the use of ports?

Reference

1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, “Computer Organization”, McGraw-Hill, 6th Edition 2012.