

SHIFT REGISTER COUNTERS

Shift Registers can be arranged to form several types of counters. Based on the type of feedback connection the shift register counters are classified as

- 1) Ring or Standard Ring Counter.
- 2) Twisted Ring or Johnson or Shift Counter.

RING COUNTER

In Ring Counter the output Q of each stage is connected to the D input of the next stage and the output of last stage is fed back to the input of first stage. The \overline{CLR} followed by \overline{PRE} makes the output of first stage to '1' and remaining outputs to '0'. Thus $Q_A = 1$ and Q_B, Q_C, Q_D are 0.

$$Q_A Q_B Q_C Q_D = 1000$$

When the first clock pulse is triggered Q_B becomes 1 remaining output are 0.

$$Q_A Q_B Q_C Q_D = 0100$$

When the second clock pulse is triggered Q_C becomes 1 and remaining outputs are 0.

$$Q_A Q_B Q_C Q_D = 0010$$

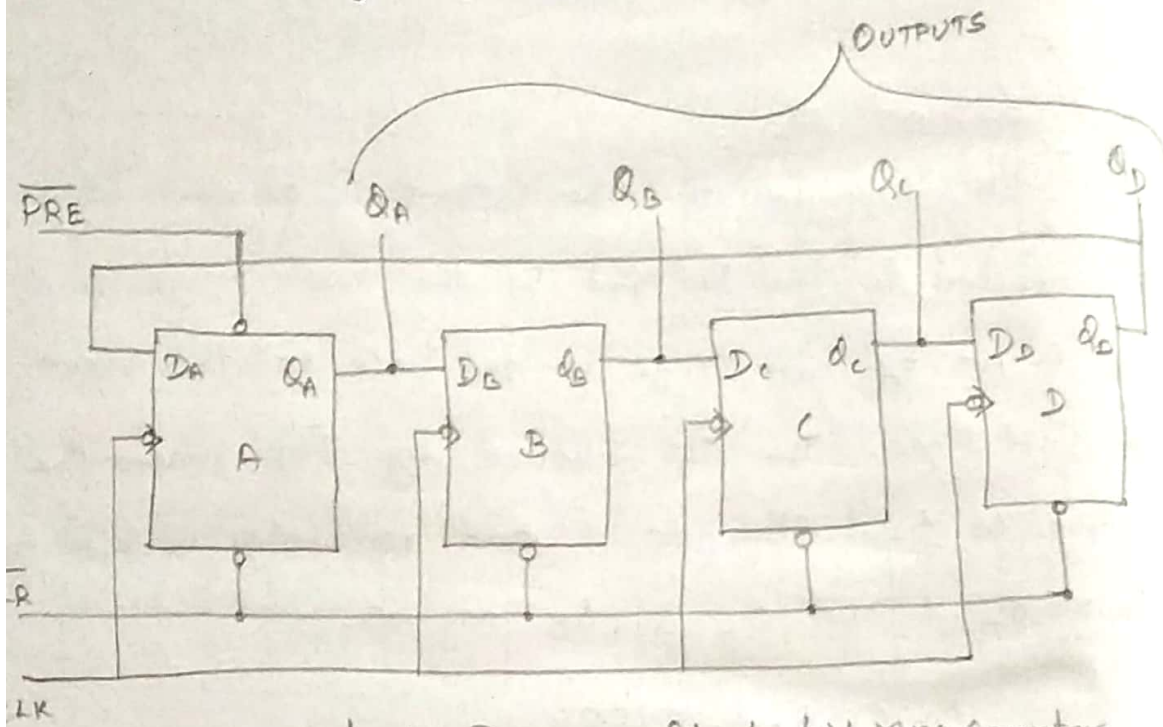
When the third clock pulse is triggered Q_D become '1' and remaining outputs are 0

$$Q_A Q_B Q_C Q_D = 0001$$

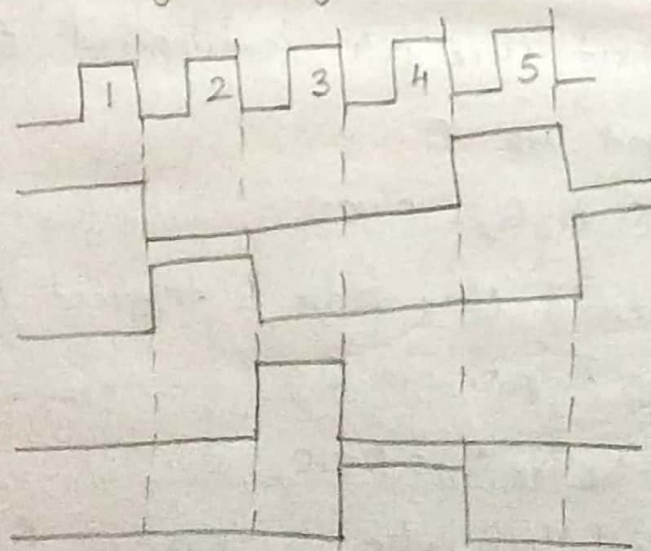
When the fourth clock pulse is triggered Q_A becomes 1 and remaining outputs are 0.

$$Q_A Q_B Q_C Q_D = 1000.$$

CLK	Q_A	Q_B	Q_C	Q_D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1



Logic Diagram of 4-bit ring counter



JOHNSON COUNTER. (Twisted Ring Counter)

In Johnson Counter the Q output of each stage of Flip-Flop is connected to D input of the next stage and the complement output \bar{Q} of the last stage is fed back to the input of first stage. The last stage output is fed back to the first stage input D_A . Initially the register is cleared. Therefore $Q_A Q_B Q_C Q_D = 0000$. Since $Q_D = 0, \bar{Q}_D = 1, D_A$ will be 1. When the first clock pulse is triggered Q_A becomes 1 and the remaining outputs are zero. Hence $Q_A Q_B Q_C Q_D = 1000$. When the second clock pulse is triggered Q_A and Q_B becomes 1 and the remaining outputs are 0. Hence $Q_A Q_B Q_C Q_D = 1100$. The change of states is shown.

CLK	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

