REGISTERS

A Flip Flop can store 1-bit of data. So an n-bit register has a group of 'n' flip flops and is capable of storing n-bit of information. Group of flip flops used to store a word is called Register.

SHIFT REGISTER

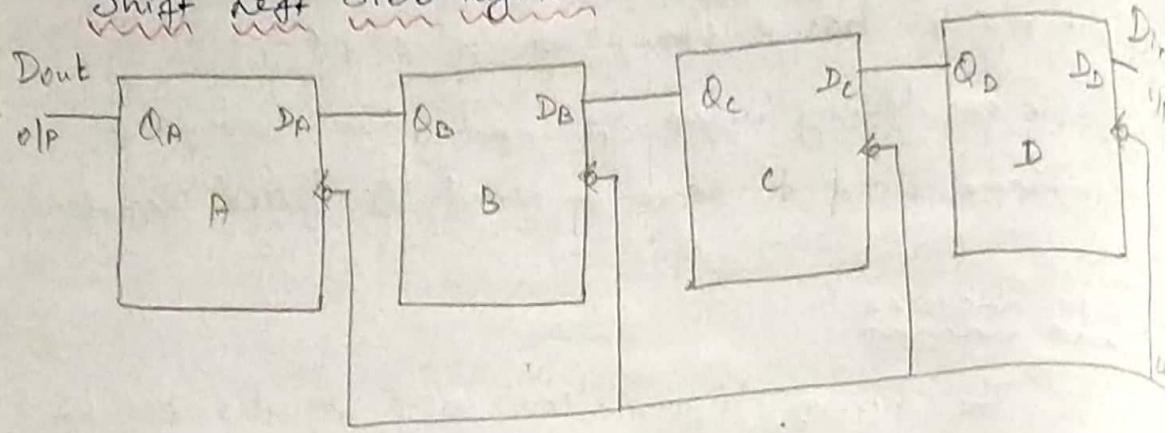
The binary information in a register can be moved from one flip-flop to another flip-flop based on the activation of clock pulses. This give rise to a group of registers called shift registers.

Based on the mode of operation shift registers are classified into

- Serial In Serial Out
- Serial In Parallel Out
- Parallel In Serial Out.
- Parallel In Parallel Out.
- Bidirectional Shift Registers.
- Universal Shift Registers.

Serial In Serial Out Shift Register (SISO)

Shift Left SISO Register.



Initially the register is cleared

$Q_A Q_B Q_C Q_D = 0000$ $\therefore$ Dout = 0

Consider the data 1111 is applied serially to Din

1) When the first negative clock edge hits, Q_D becomes '1' while Q_A, Q_B, Q_C remain '0'

$Q_A Q_B Q_C Q_D = 0001$ $\therefore$ Dout = 0

2) When the second negative clock edge hits Q_D and Q_C becomes '1' while Q_A, Q_B remain '0'.

$Q_A Q_B Q_C Q_D = 0011$ $\therefore$ Dout = 0

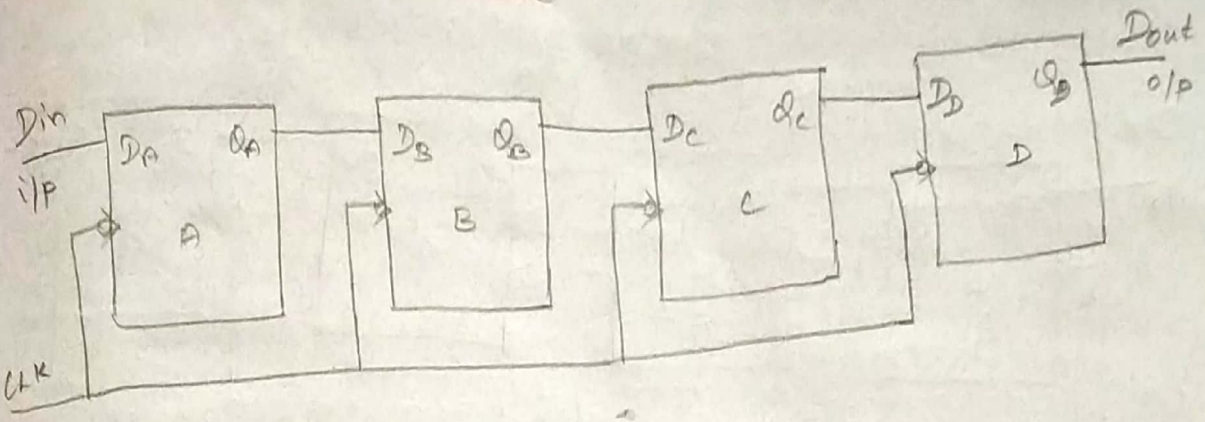
3) When the third negative clock edge hits $Q_D Q_C Q_B$ becomes '1' while Q_A remain '0'

$Q_A Q_B Q_C Q_D = 0111$ $\therefore$ Dout = 0

4) When the fourth negative clock edge hits $Q_D Q_C Q_B Q_A$ becomes '1'

$Q_A Q_B Q_C Q_D = 1111$ $\therefore$ Dout = 1

Shift Right SISO Register.



Initially the register is cleared $Q_A Q_B Q_C Q_D = 0000$

$\therefore$ Dout = 0.

Consider the data 1111 is applied serially to Din.

1) When the first negative clock edge hits Q_A becomes 1

$\therefore Q_A Q_B Q_C Q_D = 1000 \quad \therefore$ Dout = 0.

2) When the second negative clock edge hits.

$Q_A Q_B Q_C Q_D = 1100 \quad \therefore$ Dout = 0.

3) When the third negative clock edge hits.

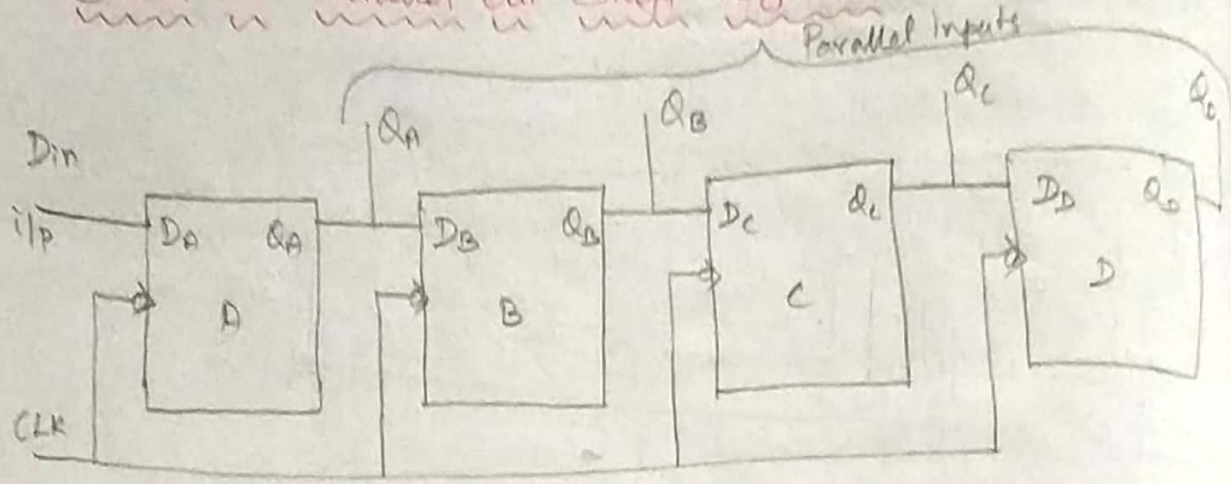
$Q_A Q_B Q_C Q_D = 1110 \quad \therefore$ Dout = 0

4) When the fourth negative clock edge hits.

$Q_A Q_B Q_C Q_D = 1111 \quad \therefore$ Dout = 1.

I/p Din	CLK	Q_A	Q_B	Q_C	Q_D	o/p Dout.
1	1	1	0	0	0	0
1	2	1	1	0	0	0
1	3	1	1	1	0	0
1	4	1	1	1	1	1

Serial In Parallel Out Shift Register. (SIPO)



Initially the Register is cleared $Q_A Q_B Q_C Q_D = 0000$

Consider the data 1111 is applied serially to Din.

when the first negative clock edge hits.

$Q_A Q_B Q_C Q_D = 1000$

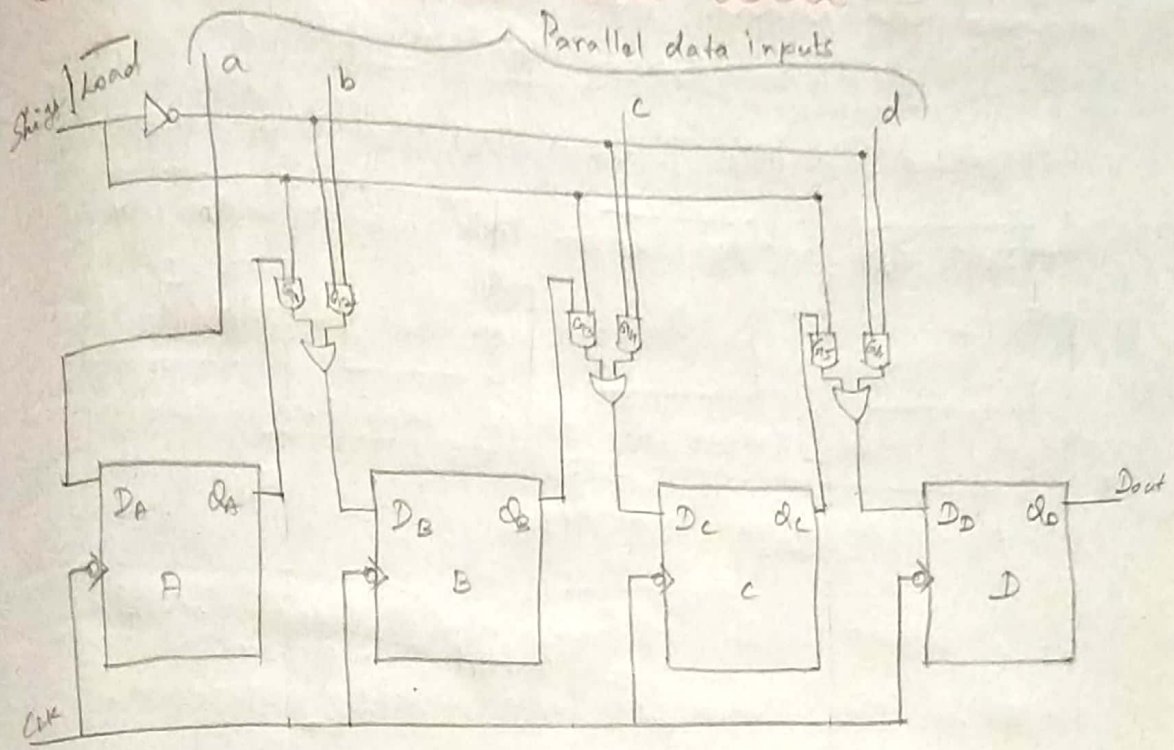
Second negative clock edge hits $Q_A Q_B Q_C Q_D = 1100$

Third negative clock edge hits $Q_A Q_B Q_C Q_D = 1110$

Fourth negative clock edge hits $Q_A Q_B Q_C Q_D = 1111$

Input Din	CLK	O/P Q_A	Q_B	Q_C	Q_D
1	1	1	0	0	0
1	2	1	1	0	0
1	3	1	1	1	0
1	4	1	1	1	1

Parallel In Serial Out Shift Register (PISO)



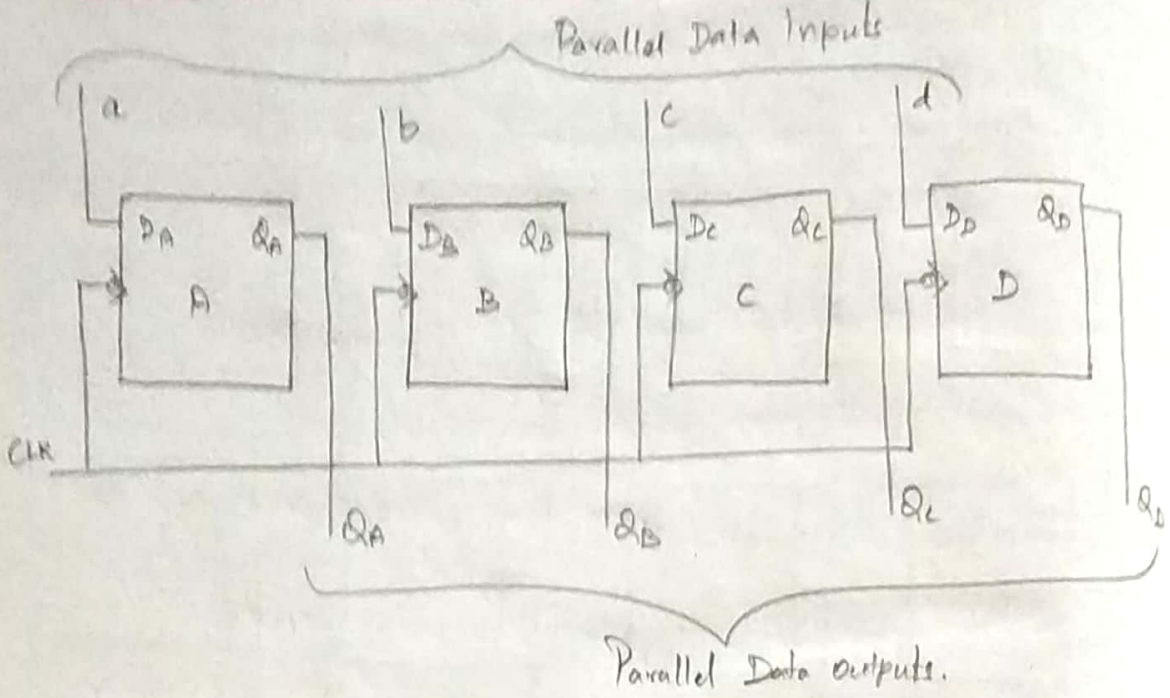
A 4-bit Parallel In Serial Out shift register has 4 inputs a, b, c and d which are entered in parallel and one serial output Dout. The control signal used here is SHIFT/$\overline{\text{LOAD}}$ which is used to select shifting or loading data operation of the register.

If SHIFT/$\overline{\text{LOAD}}$ = 0, Gates G_1, G_3, G_5 are disabled and Gates G_2, G_4, G_6 are enabled which allows the data a, b, c, d to be at D_A, D_B, D_C & D_D respectively.

When SHIFT/$\overline{\text{LOAD}}$ = 1 gates G_1, G_3, G_5 are enabled and gates G_2, G_4, G_6 are disabled. This allows the data bits to shift from one stage to the next as soon as the negative clock edge triggers.

SHIFT/$\overline{\text{LOAD}}$	I/P a	b	c	d	CLK	O/P Dout
0	1	0	1	0	–	–
1	x	x	x	x	1	0
1	x	x	x	x	2	1
1	x	x	x	x	3	0
1	x	x	x	x	4	1

Parallel In Parallel Out Shift Register (PIPO)



In PIPO Shift Registers the inputs a, b, c and d are applied to D_A, D_B, D_C and D_D respectively.

When the first negative clock edge hits $Q_A Q_B Q_C Q_D = abcd$

$Q_A = a$ $Q_B = b$. $Q_C = c$ $Q_D = d$.

Inputs				CLK	Outputs			
a	b	c	d		Q_A	Q_B	Q_C	Q_D
1	0	1	0	1	1	0	1	0
1	0	1	1	2	1	0	1	1
0	1	0	0	3	0	1	0	0
1	1	1	1	4	1	1	1	1