SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

COURSE NAME :19IT301 COMPUTER ORGANIZATION AND ARCHITECTURE

II YEAR /III SEMESTER

Unit 2-Arithmetic operations

Topic 1 : Addition and subtraction of signed numbers

II unit syllabus

Unit II	**ARITHMETIC OPERATIONS**	10
Addition and subtraction of signed numbers – Design of fast adders – Multiplication of positive numbers - Signed operand multiplication- fast multiplication – Integer division – Floating point numbers and operations		

SIGNED BIT REPRESENTATION

Representation of both *positive* and *negative* numbers

- Following 3 representations

Signed magnitude representation
Signed 1's complement representation
Signed 2's complement representation

Example: Represent +9 and -9 in 7 bit-binary number

Only one way to represent + 9 ==> 0 001001

Three different ways to represent - 9:

In signed-magnitude:	1 001001
In signed-1's complement:	1 110110
In signed-2's complement:	1 110111

Conversion

Decimal -> binary

Divide by 2	Remainder
4382	
2191	0
1095	1
547	1
273	1
136	1
68	0
34	0
17	0
8	1
4	0
2	0
1	0
0	1

4382_{ten} =
$1\ 0001\ 0001\ 1110_{two}$

Hexadecimal: base 16. Octal: base 8

$1010\ 1011\ 0011\ 1111_{two} = ab3f_{hex}$

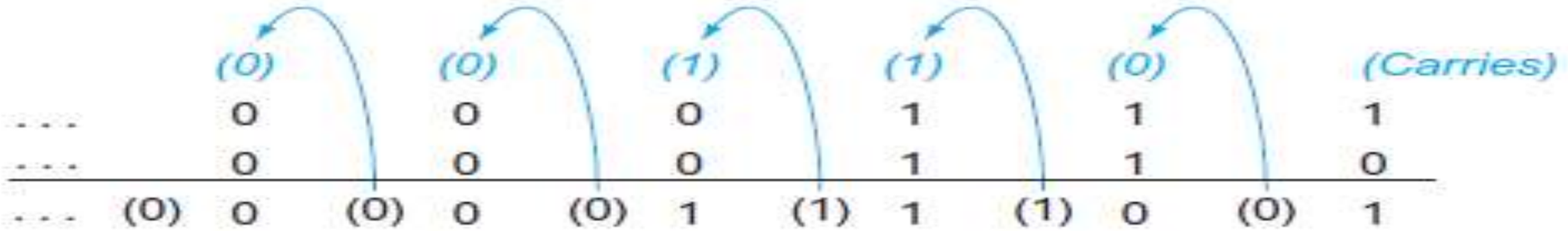
Addition and Subtraction:

Binary Addition and Subtraction

Let's try adding 6_{ten} to 7_{ten} in binary and then subtracting 6_{ten} from 7_{ten} in binary.

$$
\begin{array}{lll}
 & 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0111_{two} & = 7_{ten} \\
+ & 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0110_{two} & = 6_{ten} \\
\hline
= & 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 1101_{two} & = 13_{ten}
\end{array}
$$

The 4 bits to the right have all the action; Figure shows the sums and carries. The carries are shown in parentheses, with the arrows showing how they are passed.



Binary addition, showing carries from right to left. The rightmost bit adds 1 to 0, resulting in the sum of this bit being 1 and the carry out from this bit being 0. Hence, the operation for the second digit to the right is 0 + 1 + 1. This generates a 0 for this sum bit and a carry out of 1. The third digit is the sum of 1 + 1 + 1, resulting in a carry out of 1 and a sum bit of 1. The fourth bit is 1 + 0 + 0, yielding a 1 sum and no carry.

Subtraction:

$$
\begin{array}{ll}
 & 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0111_{two} = 7_{ten} \\
- & 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0110_{two} = 6_{ten} \\
\hline
= & 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0001_{two} = 1_{ten}
\end{array}
$$

or via addition using the two's complement representation of -6:

$$
\begin{array}{ll}
 & 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0111_{two} = 7_{ten} \\
+ & 1111\ 1111\ 1111\ 1111\ 1111\ 1111\ 1111\ 1010_{two} = -6_{ten} \\
\hline
= & 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0001_{two} = 1_{ten}
\end{array}
$$

Arithmetic Addition

Signed-magnitude Addition

- The addition of two numbers in the ***signed-magnitude*** system follows the rules of ordinary arithmetic.
- If the signs are the same, we add the two magnitudes and give the sum the common sign.
- If the signs are different, we subtract the smaller magnitude from the larger and give the result the sign of the larger magnitude.
- For example, (+25) + (-37) = -(37 - 25) = -12 and is done by subtracting the smaller magnitude 25 from the larger magnitude 37 and using the sign of 37 for the sign of the result.

Signed 2's complement addition

- The addition of two numbers in the signed 2's complement addition system follows.
- Add the two numbers, including their sign bits, and discard any carry out of the sign (leftmost) bit position. Numerical examples for addition are shown below.

Eg 1:

+6	00000110	
+13	00001101	
+19	00010011	

Eg 2:

-6	11111010	(Signed 2's complement of -6)
+13	00001101	
+7	100000111	

Eg3:

+6	00000110	
-13	11110011	(Signed 2's complement of -13)
-7	11111001	(Signed 2's complement of -7)

Eg4:

-6	11111010	(Signed 2's complement of -6)

Arithmetic subtraction

Eg 1:

-6	11111010	(Signed 2's complement of -6)
-13	11110011	(Signed 2's complement of -13)
-6	11111010	
-13	00001101	(2's complement of -13)
+7	1] 00000111	

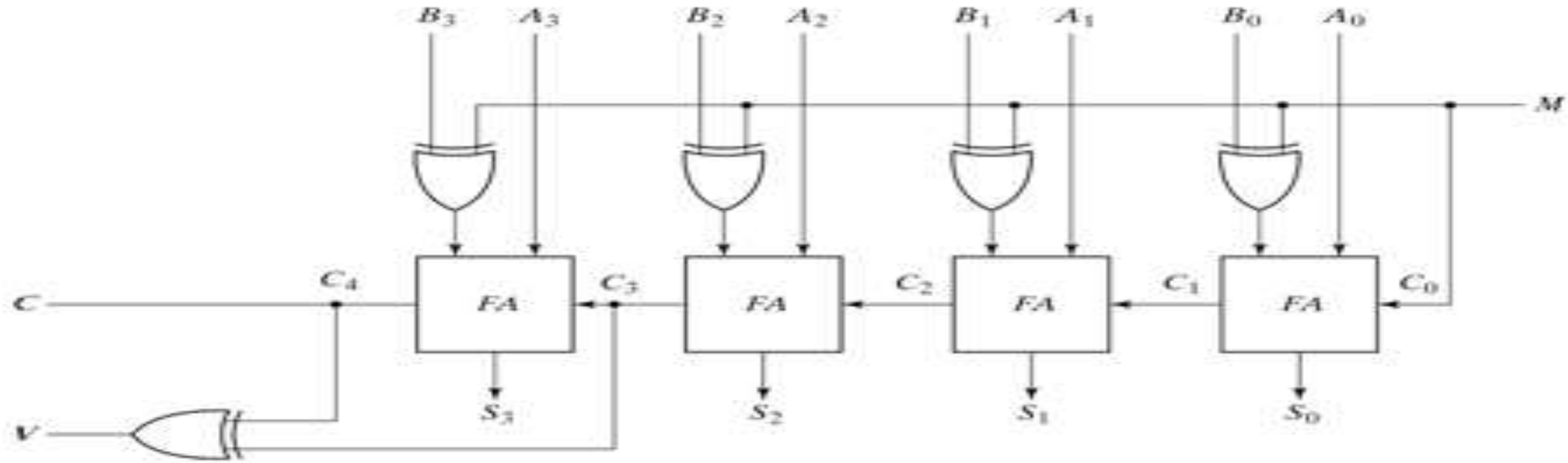
Eg 2:

+13	00001101	
+6	00000110	
+13	00001101	
+6	11111010	(2's complement of +6)
+7	1] 00000111	

Eg 3:

-6	11111010	(Signed 2's complement of -6)
+13	00001101	
-6	11111010	
+13	11110011	(2's complement of +13)
-19	1] 11101101	

Four Bit Adder-Subtractor:



4-Bit Adder Subtractor

Overflow conditions for addition and subtraction

✓overflow occurs when adding two positive numbers and the sum is negative, or vice versa. This means a carry out occurred into the sign bit.

✓Overflow occurs in subtraction when we subtract a negative number from a positive number and get a negative result, or when we subtract a positive number from a negative number and get a positive result. This means a borrow occurred , from the sign bit.

Assessment

a). What is signed number?_____

_____

_____

b) Mention the purpose

1.ALU unit_____

2. Adder circuit _____

3.Adder/subtracor _____

Reference

1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, “Computer Organization”, McGraw-Hill, 6th Edition 2012.