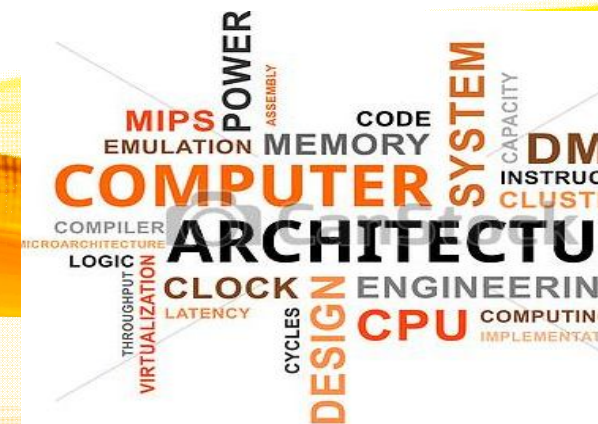


# UNIT II

## ARITHMETIC OPERATIONS

Addition and subtraction of signed numbers – Design of fast adders –  
Multiplication of positive numbers - Signed operand multiplication- **fast multiplication** – Integer division – Floating point numbers and operations



# Recap the previous Class





## a) Bit-Pair Recoding of Booth's Multiplication

–A technique that halves the maximum number of summands; derived directly from the Booth's algorithm.

–If we **group the Booth-coded multiplier digits in pairs**, we observe:

$$(+1, -1): (+1, -1) * M = 2 * M - M = M$$

$$(0, +1): (0, +1) * M = M$$

–We need a single addition instead of a pair of addition & subtraction.

•Other similar rules can be framed.



# Design of Fast Multiplier

Original Booth-coded Pair	Equivalent Recoded Pair
(+1, 0)	(0, +2)
(-1, +1)	(0, -1)
(0, 0)	(0, 0)
(0, 1)	(0, 1)
(+1, 1)	--
(+1, -1)	(0, +1)
(-1, 0)	(0, -2)

- Every equivalent recoded pair has at least one 0.
- Worst-case number of additions or subtractions is 50% of the number of multiplier bits.
- Reduces the worst-case time required for multiplication.



## Example: (+13) X (-22) in 6-bits.

Original:	Multiplier --	1	0	1	0	1	0
Booth:	Multiplier --	-1	+1	-1	+1	-1	0
Recoded:	Multiplier --	0	-1	0	-1	0	-2

	0	0	1	1	0	1	
	.	-1	.	-1	.	-2	
-----							
1	1	1	1	1	1	1	0
							0 1 1 0
	1	1	1	1	1	0	0 1 1
	1	1	1	0	0	1	1
-----							
1	1	0	1	1	1	0	0 0 1 0

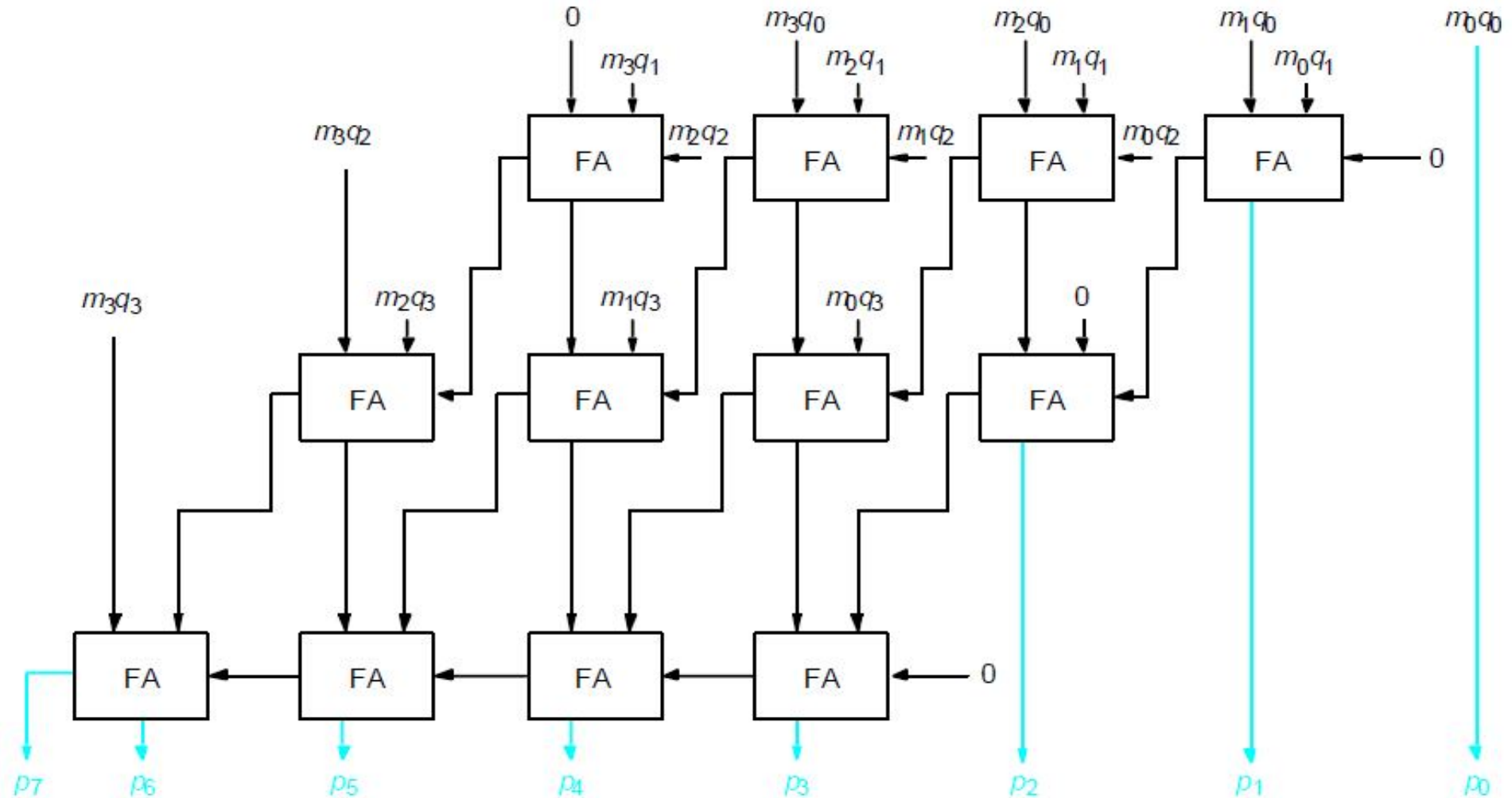
- $M = 001101 (+13)$
- $-1 * M = 110011$
- $-2 * M = 100110$

## b) Carry Save Multiplier

- We have seen earlier how carry save adders (CSA) can be used to add several numbers with carry propagation only in the last stage.
- The partial products can be generated in parallel using  $n^2$  AND gates.
- The  $n$  partial products can then be added using a CSA tree.
- Instead of letting the carries ripple through during addition, we *save* them and feed it to the next row, at the correct weight positions.



# 4 x 4 Carry Save Multiplier

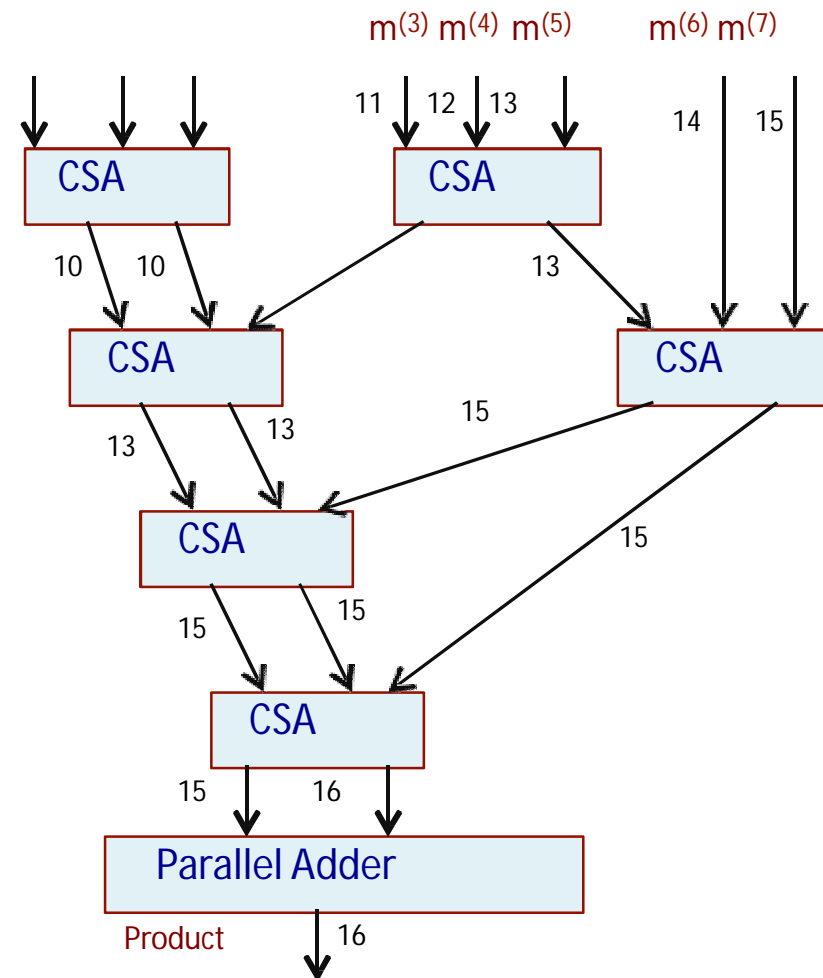


# Wallace Tree Multiplier

- A Wallace tree is a circuit that **reduces the problem of summing  $n$   $n$ -bit numbers** to the problem of summing two  $\Theta(n)$ -bit numbers.
- It uses  $n/3$  (floor of) carry-save adders in parallel to convert the sum of  $n$  numbers to the sum of  $2n/3$  (ceiling of) numbers.
- It then recursively constructs a Wallace tree on the  $2n/3$  (ceiling of) resulting numbers.
- The set of numbers is progressively reduced until there are only two numbers left.
- By performing many carry-save additions in parallel, Wallace trees allow two  $n$ -bit numbers to be multiplied in  $\Theta(\log_2 n)$  time using a circuit of size  $\Theta(n^2)$ .



- The figure shows a Wallace tree that adds 8 partial products  $m^{(0)}$ ,  $m^{(1)}$ , ...,  $m^{(7)}$ .
- The partial product  $m^{(i)}$  consists of  $(n+i)$  bits.
- Each line represents an entire number – the label of an edge indicates the number of bits.
- The carry-lookahead adder at the bottom adds a  $(2n-1)$ -bit number to a  $2n$ -bit number to give the  $2n$ -bit product.





## TEXT BOOK

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4. M. Morris R. Mano "Computer System Architecture" 3rd Edition 2007
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# THANK YOU