SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

COURSE NAME :19IT301 COMPUTER ORGANIZATION AND ARCHITECTURE

II YEAR /III SEMESTER

Unit 1- **BASIC STRUCTURE OF COMPUTERS**

Topic 8: Addressing modes

Addressing modes

1.Immediate addressing

The operand is given explicitly in the instruction

Add #6,R1 R1 <-6+R1

2.Register addressing

The operand is the contents of a processor register in the instruction

Add R3,R4 R4 <- R4 + R3

3. Absolute(direct address)

Address of the operand is in the instruction

Add B,R4 R4 <- R4 + B

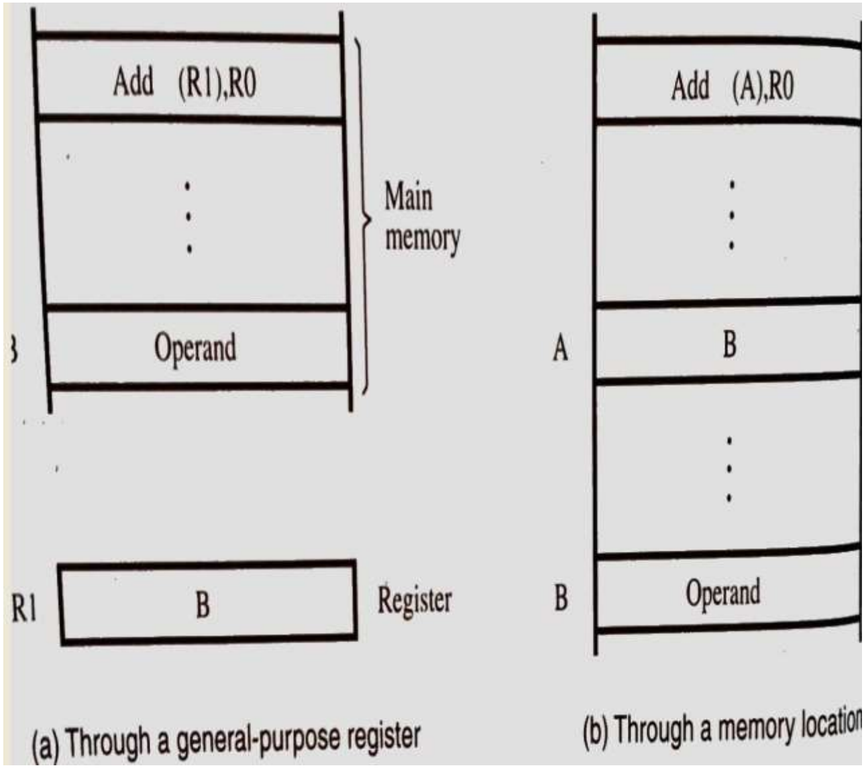
Addressing modes

4. Indirect

The address of the operand is the contents of a register or memory location whose address appears in the instruction.

Add (R1),R0 R0 <-R0+M[M[R1]]

Add (A),R0 R0 <- R0+M[M[A]]



Addressing modes

5. Index addressing

The effective address of the operand is generated by adding a constant value to contents of a register.

Add 20(R1),R2 R2<- R2 +M[20+R1]

6. Base with index addressing

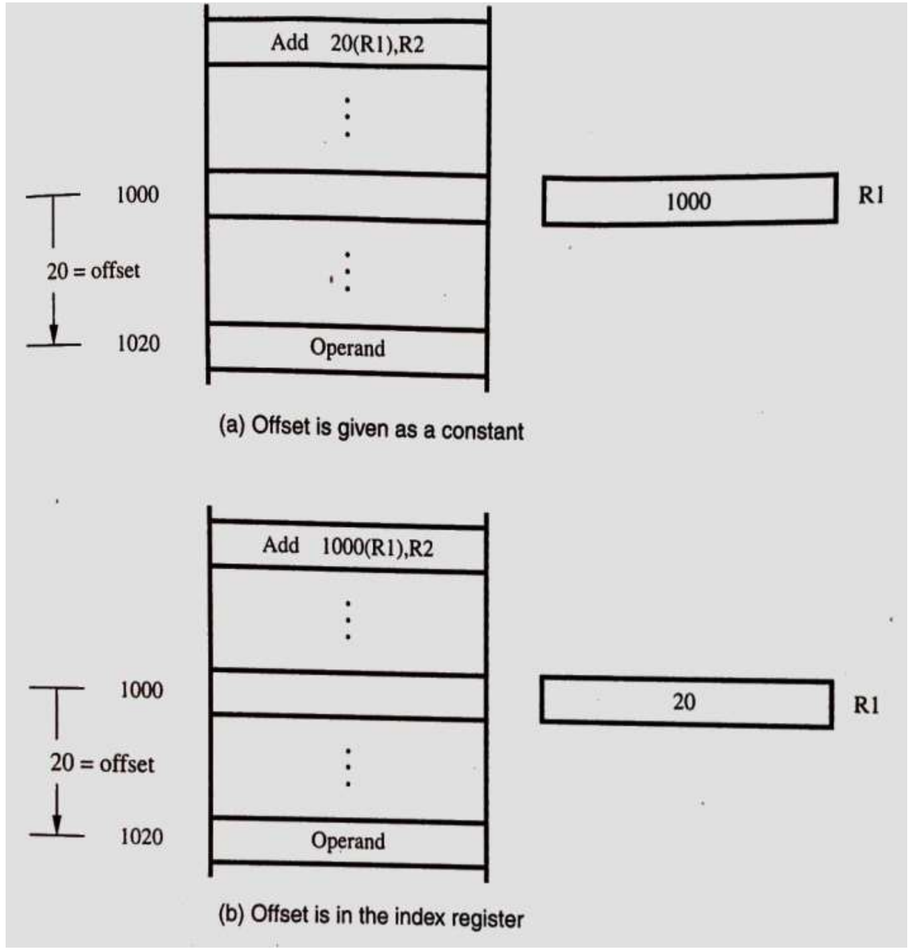
Add (R1 + R2), R4 R4 <- R4 + M[R1 + R2]]

#R2 base register, R1 index register

7. Base with index and offset addressing

Add 6(R1 + R2), R4 R4 <- R4 + M[6+R1 + R2]

#R2 base register, R1 index register

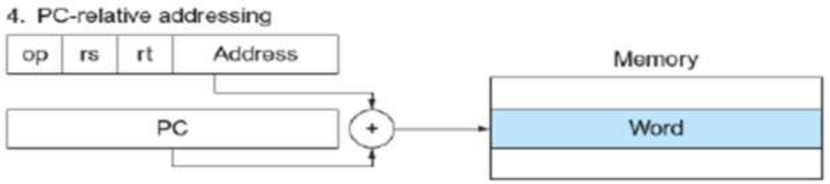


Addressing modes

8. The relative mode: X(PC) EA=[PC]+X

The effective address is determined by the index mode using the PC in place of the general purpose register Ri

X= -16



9. Autoincrement mode – the effective address of the operand is the contents of a register specified in the instruction. After accessing the operand, the contents of this register are automatically incremented to point to the next item in a list. Add (R2)+, R0

(R_i)+. The increment is 1 for byte-sized operands, 2 for 16-bit operands, and 4 for 32-bit operands.

10 Autodecrement mode: -(R_i) decrement first

	100	Move	N,R1
	104	Move	#NUM1,R2
	108	Clear	R0
LOOP	112	Add	(R2),R0
	116	Add	#4,R2
	120	Decrement	R1
	124	Branch>0	LOOP
	128	Move	R0,SUM
	132		
		⋮	
SUM	200		
N	204	100	
NUM1	208		
NUM2	212		
		⋮	
NUM*n*	604		

Addressing modes

	Addressing Mode	Example	Action	
1.	Register	Add R3,R4	R4 <- R4 + R3	
2.	Immediate	Add #3,R4	R4 <- R4 + 3	
3.	Register indirect	Add (R1),R4	R4 <- R4 + M[R1]	
4.	Indexed	Add 5(R3), R4	R4 <- R4 + M[R3 + 5]	
5.	Base with index	Add (R1 + R2), R4	R4 <- R4 + M[R1 + R2]	#R2 base register
6.	Base with index and offset	Add 6(R1 + R2), R4	R4 <- R4 + M[6+R1 + R2]	#R2 base register
7.	Direct	Add LOC,R4	R4 <- R4 + LOC	
8.	Memory Indirect	Add (LOC),R4	R4 <- R4 + M[M[LOC]]	
9.	Relative	X(PC)	EA= X+ [PC]	
10.	Autoincrement	Add (R2)+ ,R4	R4 <- R4 + M[R2]	R2 <- R2 + 4 (in case of 32 bit word length)
	Autodecrement	Add (R2)-, R4	R4 <- R4 + M[R2]	R2 <- R2 - d

CTS test pattern

Cognizant Test pattern for Programmer Analyst Trainee (on campus)

Cognizant recruits in large number for this role each year from various colleges. The CTS test pattern for the Cognizant online test (first round) is as below.

Sections	Number of questions	Duration
Quantitative Aptitude	16	16 mins
Logical Reasoning	24	35 mins
Verbal Ability	22	18 mins
Automata fix	7	20 mins

Click Here to Know Automata Fix Sample Questions

The next round will a Face to Face Technical interview round and followed by HR round. For detailed information of Cognizant Recruitment process 2020, check here.

Quantitative Aptitude	Time and work Ratios and Proportion Averages, Profit & Loss Time, speed and distance Percentages Permutations and Combinations Probability Logarithms Geometry
Logical Reasoning	Data Arrangements Blood Relations Coding and Decoding series Analogy Odd man out Data Sufficiency Direction Sense Logical Sequence
Verbal Ability	Reading Comprehension Para-Jumbles Sentence Completion Sentence improvement Sentence Correction Vocabulary
Automata Fix	Logical Error Correction Syntax Error Correction Code Reuse

Assessment

a). What are the types of addressing modes?_____

_____

_____

b) Give the purpose of the following:

1.PC relative addressing_____

2. Immediate addressing____

3. Indexed addressing _____

Reference

1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, “Computer Organization”, McGraw-Hill, 6th Edition 2012.