# SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

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## DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

## COURSE NAME :19IT301 COMPUTER ORGANIZATION AND ARCHITECTURE

II YEAR /III SEMESTER

Unit 1- **BASIC STRUCTURE OF COMPUTERS**

Topic 3 : Bus structures
Topic 4: Performance

# Bus structures

- A group of lines that serves as a connecting path for several devices is called a *bus*.
- Address bus
- Data bus
- Control bus

# Bus structures

1. Since the bus can be used for only one transfer at a time, only two units can actively use the bus at any given time.
2. Bus control lines are used to arbitrate multiple requests for use of one bus.
3. Single bus structure is
   - ✓ Low cost
   - ✓ Very flexible for attaching peripheral devices
4. Multiple bus structure certainly increases the performance but also increases the cost significantly.

# bus structures

- ✓Different devices have different transfer/operate speed.
- ✓If the speed of bus is bounded by the slowest device connected to it, the efficiency will be very low.

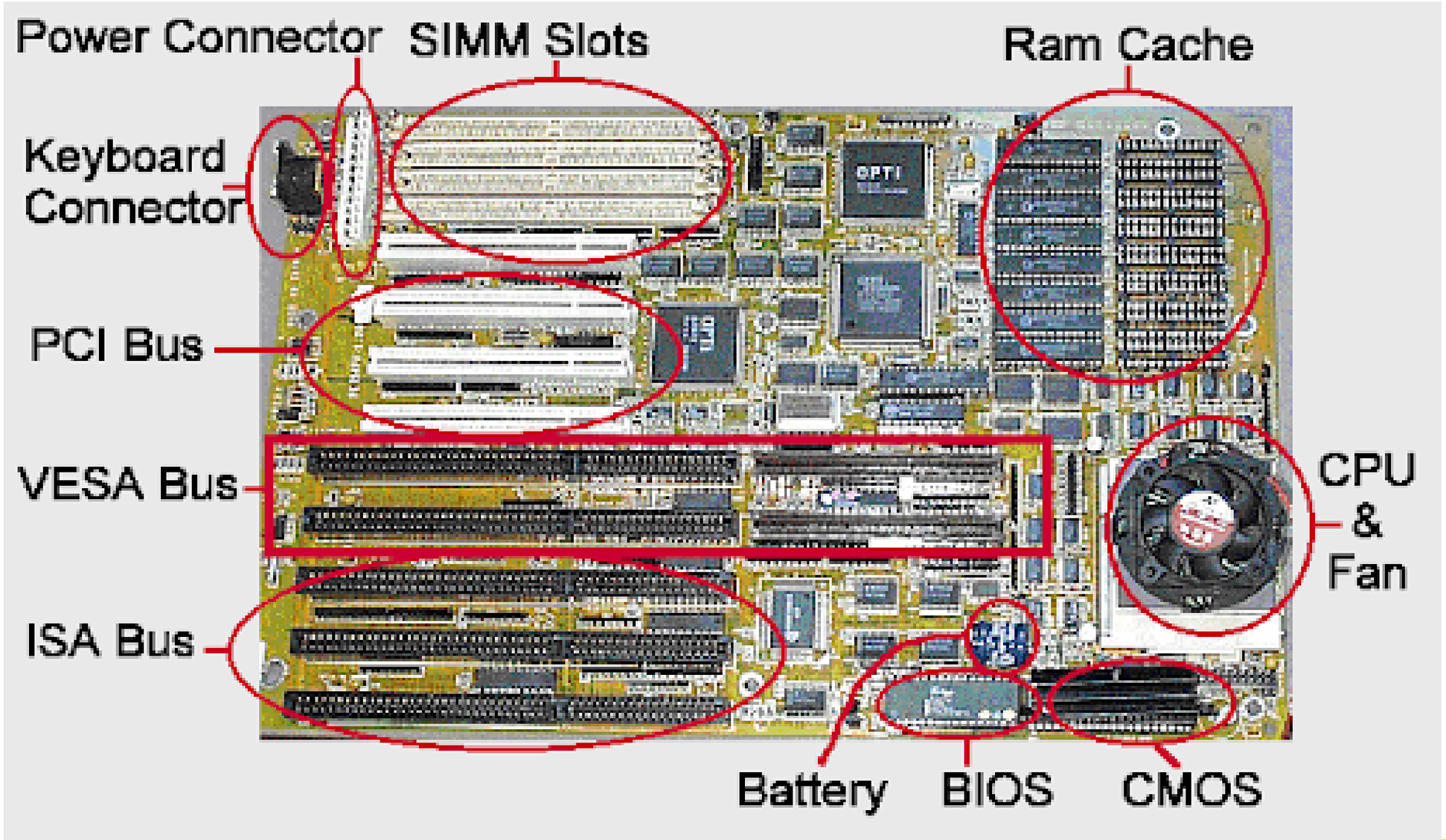
How to solve this?

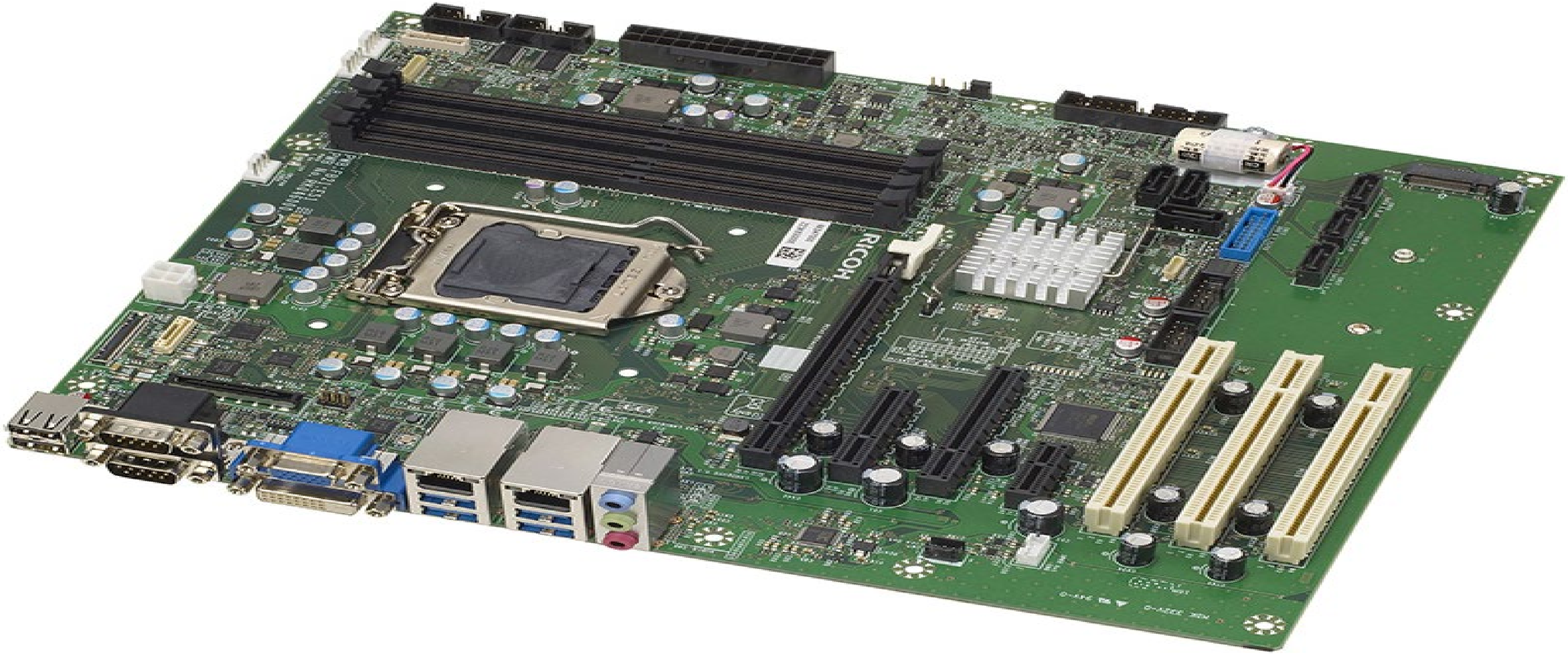
- ✓A common approach – use buffers.
- ✓The instructions from the processor at once are loaded into these buffers and then the complete transfer of data to the slow speed device.

Buses in PC

- ✓PCI- Peripheral component Interconnect
- ✓VESA-Video Electronics Standards Association
- ✓ISA- Industry standard architecture
- ✓AGP- Accelerated graphics port

# Bus structures




RICOH

# Assessment

a). What is Multi Bus?

_____

_____

_____

b) Mention the purpose

1.Address bus_____

2. Data bus ____

3.Control bus _____

4.buffers _____

5. Single bus _____

# Performance

The most important measure of a computer is how quickly it can execute programs with high accuracy and efficiency.

Three factors affect performance:

- Hardware design
- Instruction set
- Compiler

# Performance

Processor time to execute a program depends on the hardware involved in the execution of individual machine instructions.

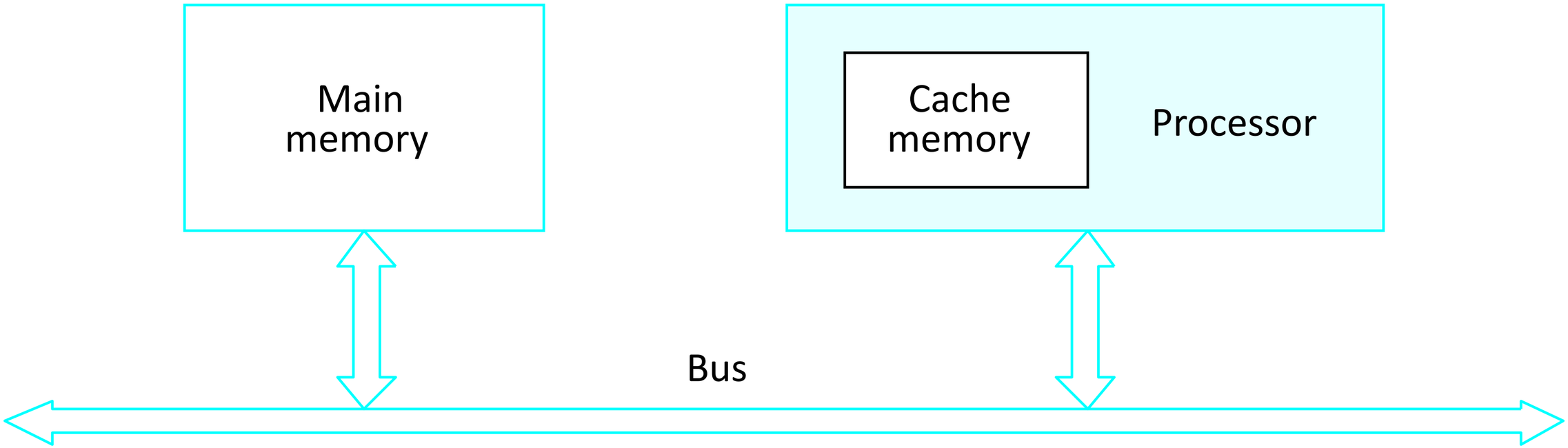



Figure 1 The processor cache.

# Performance

The processor and a relatively small cache memory can be fabricated on a single integrated circuit chip.

✓Speed

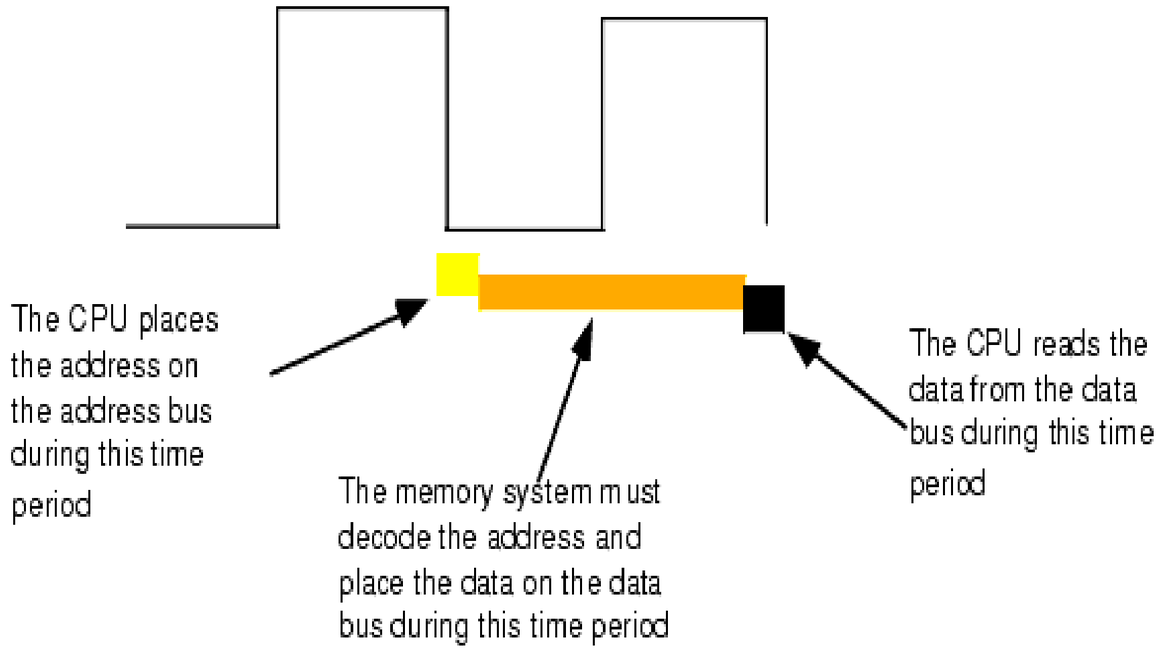
✓Cost

✓Memory management

# Performance -Processor Clock

Clock, clock cycle, and clock rate

The execution of each instruction is divided into several steps, each of which completes in one clock cycle.



# Performance –Basic performance equation

- ✓T – processor time required to execute a program that has been prepared in high-level language
- ✓N – number of actual machine language instructions needed to complete the execution (note: loop)
- ✓S – average number of basic steps needed to execute one machine instruction. Each step completes in one clock cycle
- ✓R– Clock rate

$$T = \frac{N \times S}{R}$$

## How to improve T?

- ➢R – Increase R by IC technology
- ➢N– Reduce N by ISA, micro architecture and compiler
- ➢S– Reduce S by ISA and compiler

# Performance –Basic performance equation

- ✓High level language
- ➢C=A+B
- ✓Assembly language
- ➢Add R4, R5, R6
- ➢basic steps needed to execute Add R4, R5, R6

| Step | Action |
|---|---|
| 1 | $PC_{out}$, R=B, $MAR_{in}$, Read, IncPC |
| 2 | WMFC |
| 3 | $MDR_{outB}$, R=B, $IR_{in}$ |
| 4 | $R4_{outA}$, $R5_{outB}$, SelectA, Add, $R6_{in}$, End |

Control sequence for the instruction. Add R4,R5,R6,
for the three-bus organization

# Performance -Pipeline and Superscalar Operation

- ✓Instructions are not necessarily executed one after another.
- ✓Pipelining – overlapping the execution of successive instructions.

- ✓Superscalar operation – multiple instruction pipelines are implemented in the processor.
- ✓Goal – reduce S

$$T = \frac{N \times S}{R}$$

# Performance - compiler

- ✓A compiler translates a high-level language program into a sequence of machine instructions.
- ✓To reduce N, we need a suitable machine instruction set and a compiler that makes good use of it.
- ✓Goal – reduce N×S
- ✓A compiler may not be designed for a specific processor; however, a high-quality compiler is usually designed for, and with, a specific processor.

# Performance Measurement

✓T is difficult to compute.

✓Measure computer performance using benchmark programs.

✓System Performance Evaluation Corporation (SPEC) selects and publishes representative application programs for different application domains, together with test results for many commercially available computers.

✓Compile and run (no simulation)

$$SPEC\ rating = \frac{\text{Running time on the reference computer}}{\text{Running time on the computer under test}}$$

$$SPEC\ rating = \left(\prod_{i=1}^{n} SPEC_i\right)^{\frac{1}{n}}$$

n= number of programs

# Performance Measurement

If the SPEC rating = 50  means that computer under test is 50 times as fast as the reference computer

# Assessment

a). What is Basic performance equation?

_____

_____

_____

b) What are the three factors affect performance:

1..____

2. ____

3. _____

# Reference

1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, “Computer Organization”, McGraw-Hill, 6th Edition 2012.