



# **SNS COLLEGE OF ENGINEERING**



**Kurumbapalayam(Po), Coimbatore – 641 107**

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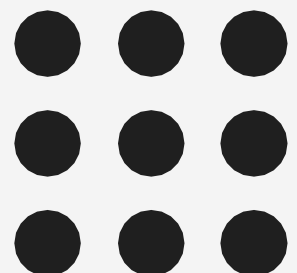
## **Department of Information Technology**

**Course Name – 19IT301 Computer Organization and  
Aechitecture**

**II Year / III Semester**

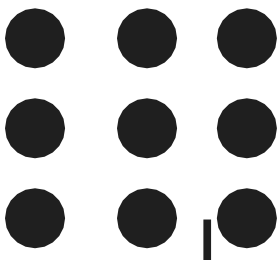
**Unit 1 – Basic Structures of Computers**

**Topic :Performance**





# Performance



- The processor and a relatively small cache memory can be fabricated on a single integrated circuit chip.
- Speed
- Cost
- Memory management



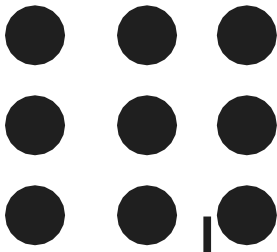
# Processor Clock



- Clock, clock cycle, and clock rate
- The execution of each instruction is divided into several steps, each of which completes in one clock cycle.
- Hertz – cycles per second



# Processor Clock



- T – processor time required to execute a program that has been prepared in high-level language
- N – number of actual machine language instructions needed to complete the execution (note: loop)
- S – average number of basic steps needed to execute one machine instruction. Each step completes in one clock cycle
- R – clock rate



# Pipeline and Superscalar Operation



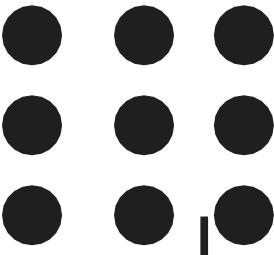
Instructions are not necessarily executed one after another.

- The value of  $S$  doesn't have to be the number of clock cycles to execute one instruction.
- Pipelining – overlapping the execution of successive instructions.
- Add R1, R2, R3
- Superscalar operation – multiple instruction pipelines are implemented in the processor.



# Clock Rate

- Improve the integrated-circuit (IC) technology to make the circuits faster
- Reduce the amount of processing done in one basic step
- Increases in  $R$  that are entirely caused by improvements in IC technology affect all aspects of the processor's operation equally except the time to access the main memory.





# Compiler



- A compiler translates a high-level language program into a sequence of machine instructions.
- To reduce  $N$ , we need a suitable machine instruction set and a compiler that makes good use of it.
- Goal – reduce  $N \times S$
- A compiler may not be designed for a specific processor; however, a high-quality compiler is usually designed for, and with, a specific processor.



# CISC and RISC



- Tradeoff between  $N$  and  $S$
- A key consideration is the use of pipelining
- $S$  is close to 1 even though the number of basic steps per instruction may be considerably larger
- It is much easier to implement efficient pipelining in processor with simple instruction sets.





# Performance Measurement



- T is difficult to compute.
- Measure computer performance using benchmark programs.
- System Performance Evaluation Corporation (SPEC) selects and publishes representative application programs for different application domains, together with test results for many commercially available computers.
- Compile and run (no simulation)
- Reference computer

$$SPEC\ rating = \frac{\text{Running time on the reference computer}}{\text{Running time on the computer under test}}$$

$$SPEC\ rating = \left( \prod_{i=1}^n SPEC_i \right)^{\frac{1}{n}}$$



**THANK YOU**