SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

19ECT221 – MICROPROCESSORS AND MICROCONTROLLERS

II YEAR - IV SEM

UNIT 2 – LED Display

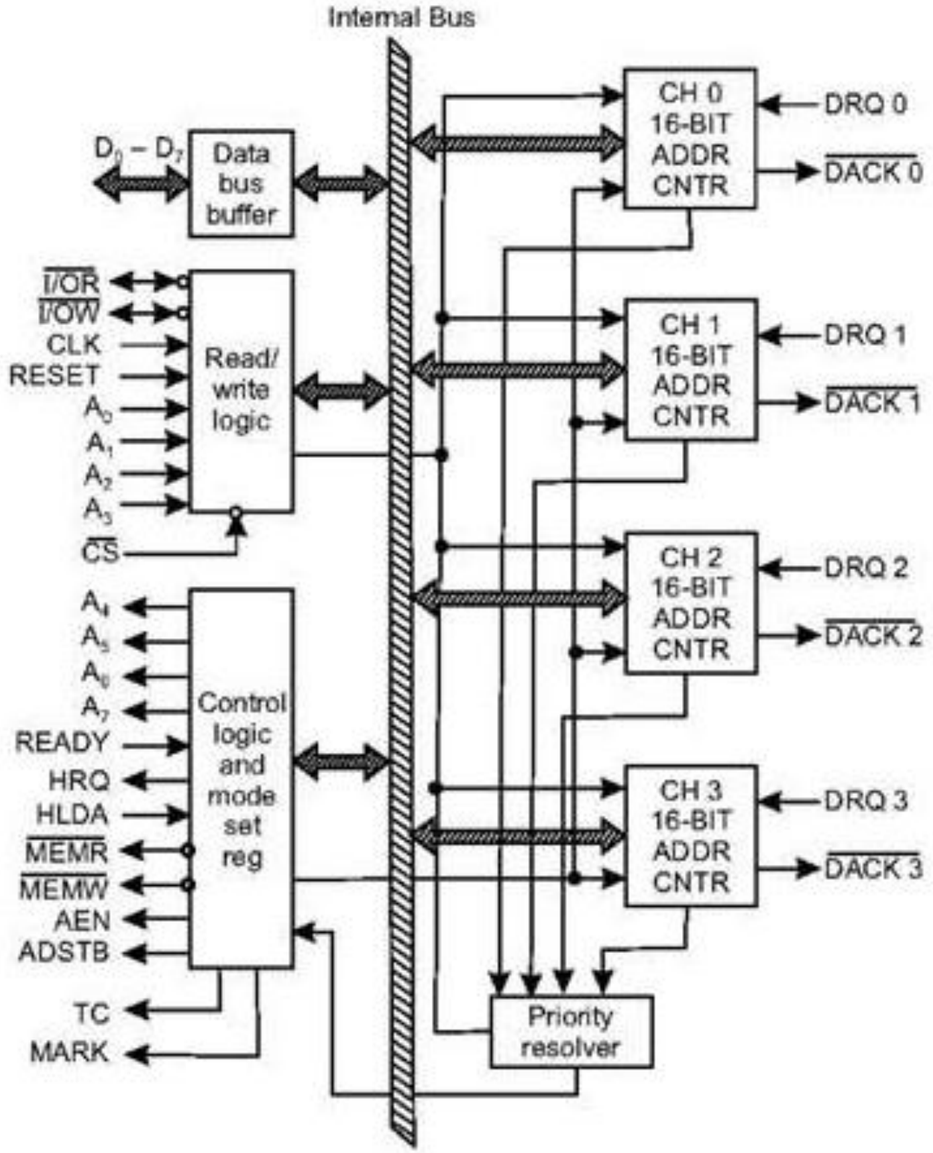
I/O Interfacing- LED Display

- We interface the I/O device in a very segmented manner and is carried systematically.
- In the interfacing of seven segment display to 8085 microcontroller it is found that An output device which is very common is, especially in the kit of 8085 microprocessor and it is the Light Emitting Diode consisting of seven segments.
- Moreover, we have eight segments in a LED display consisting of 7 segments which includes‘.’, consisting of character 8 and having a decimal point just next to it.
- We denote the segments as ‘a, b, c, d, e, f, g, and dp’ where dp signifies ‘.’ which is the decimal point resulting to a seven display circuit of LEDs which are seven segmented now the display is visual to the serial transfer of 8085 microcontroller

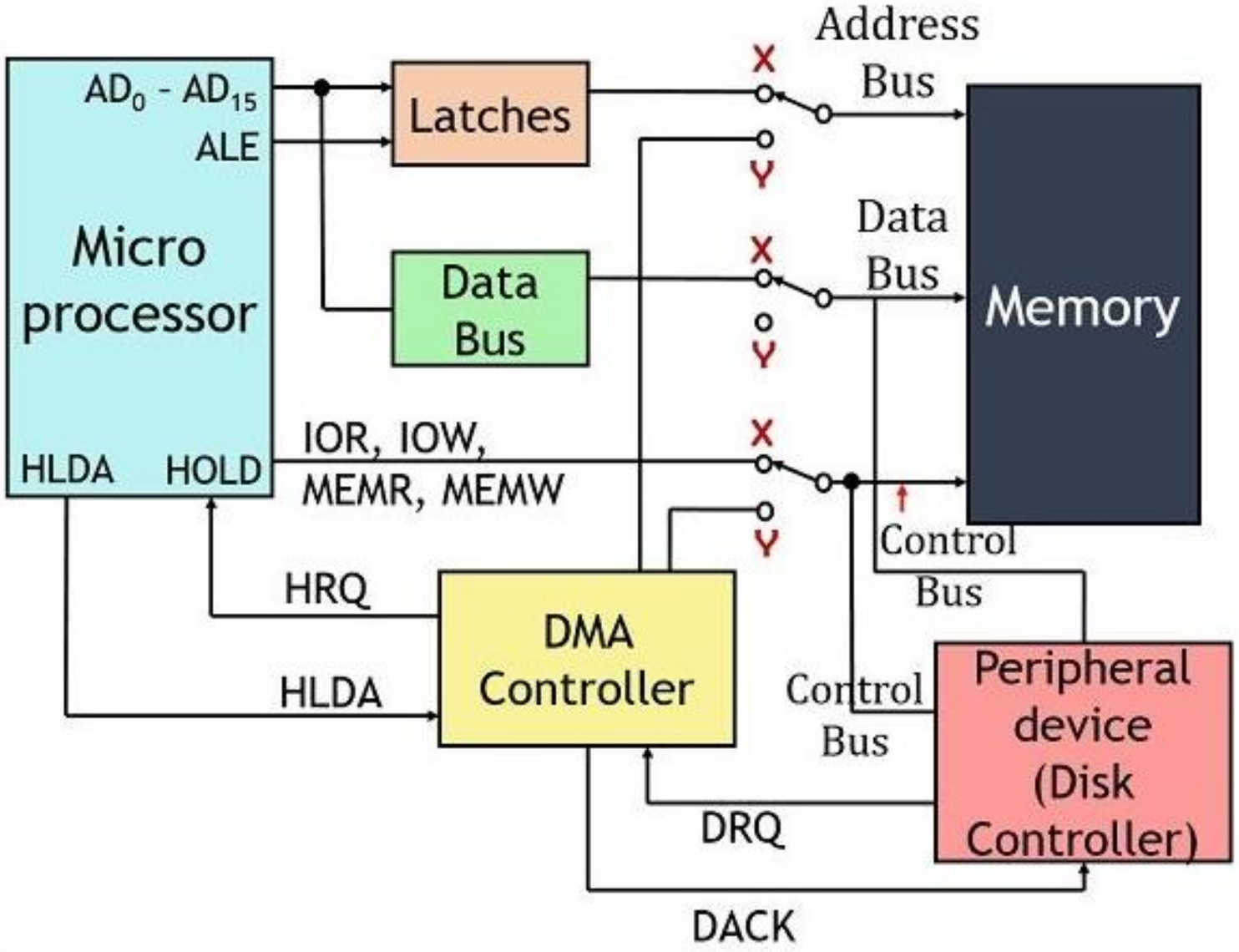
Sequence of DMA Operation

- Initially, the device has to send DMA request (DRQ) to DMA controller.
- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.
- Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU leaves the control over bus and acknowledges the HOLD request through HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the CPU, memory, and I/O devices.

Architecture of 8257

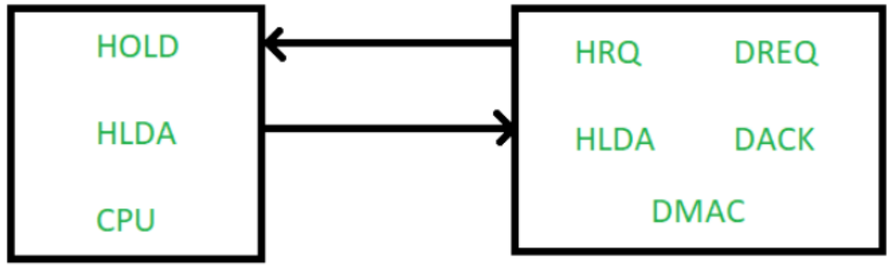


Architecture of 8257

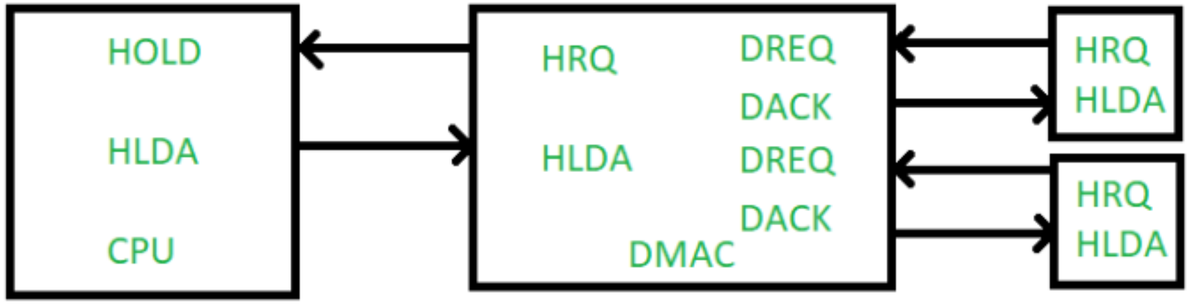


Modes of DMAC

1. Single Mode – In this only one channel is used, means only a single DMAC is connected to the bus system.



2. Cascade Mode – In this multiple channels are used, we can further cascade more number of DMACs.



Features of 8257

- Four independent DMA channels
- **Address and Data Bus-** Separately available for DMA
- **Burst Mode Transfer –** transfer the data blocks quickly
- **Priority Schemes –** Assign priorities based on the device preferance
- **Auto Initialization-** automatically reload the DMA address and count register after every transfer.
- **Compatible with diff processor-** with 8085, 8086, z80

References

https://www.tutorialspoint.com/microprocessor/microprocessor_8257_dma_controller.htm

https://electronicsdesk.com/dma-controller.html

Ramesh S.Gaonkar," Microprocessor – Architecture, Programming and Applications with the 8085", Penram International Publisher,7th Ed., 2016