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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ITT204 - MICROCONTROLLER AND EMBEDDED SYSTEMS

II YEAR/ IV SEMESTER

UNIT III EMBEDDED SYSTEM CONCEPTS AND PROCESSORS

TOPIC – 8051 Microcontroller -Functional Block Diagram

The 8051 Architecture consist of these specific features

- The 8 bit CPU with Registers A and B
- Internal ROM
- 16-bit program counter(PC) and data pointer(DPTR)
- Internal RAM of 128 bytes
- 8-bit Program Status word(PSW)
- Two 16 bit Counter / timers
- 4 eight-bit ports
- 3 internal interrupts and 2 external interrupts.
- Control register
- Oscillator and clock circuits.

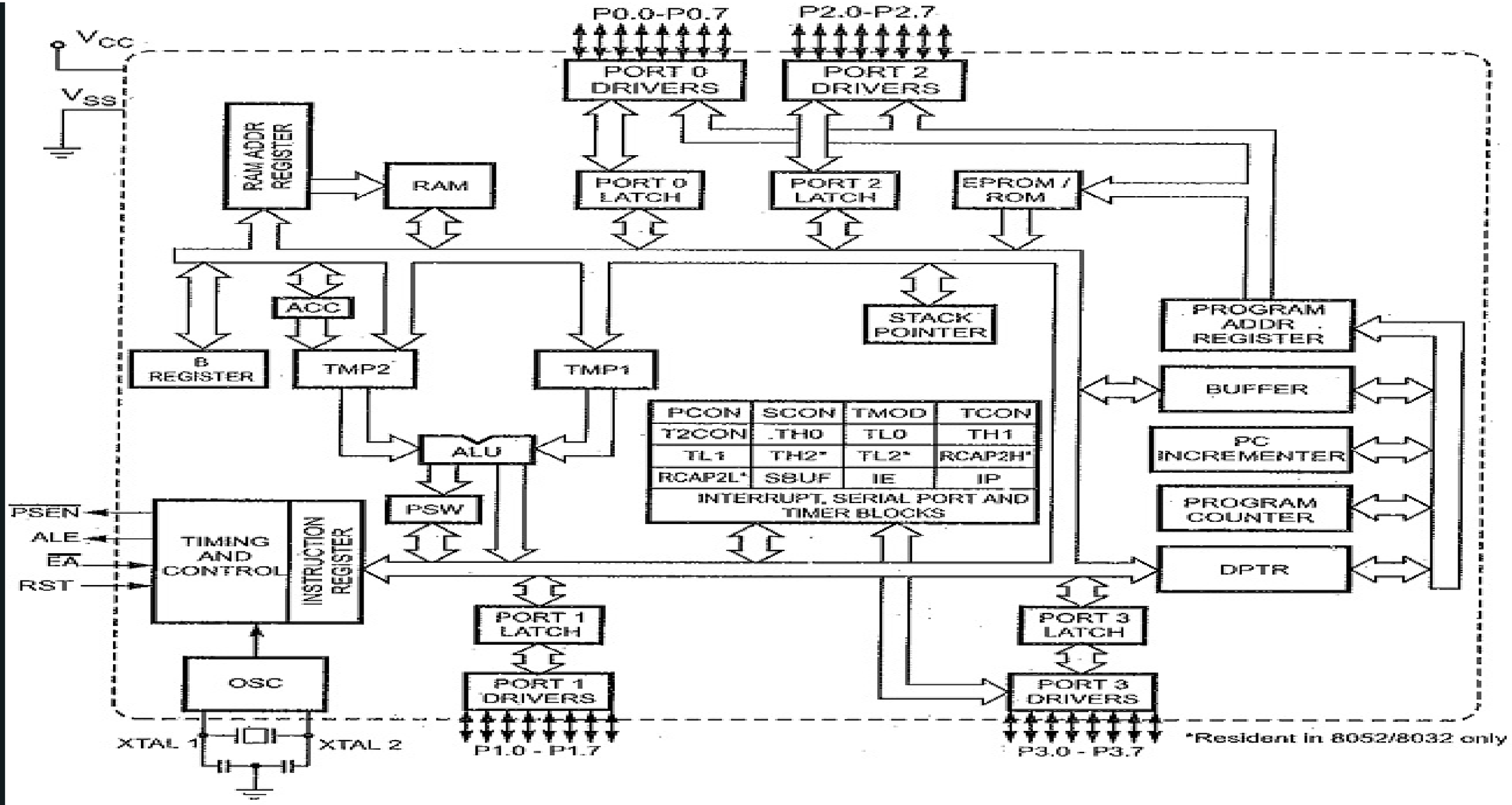


Fig. 12.2 Intel 8051/8031 architecture

A and B CPU Register

- The 8051 contains 34 general purpose or working registers. Two of these Register A and B.
  - The immediate result is stored in the accumulator register (Acc) for next operation.
  - The B register is a register just for multiplication and division operation which requires more register spaces for the product of multiplication and the quotient and the remainder for the division.

Program status word(PSW)

- The program status word shown in figure.
- The PSW contain the math flags, User program flag F0,and the register select bits that identify which of the four General-purpose register banks is currently in use by the program.
- The math flags include carry(c),auxiliary carry(AC), overflow(OV) and parity(p)

Program Status Word (PSW)

The PSW register contains several status bits that reflect the current state of the CPU.

CY	AC	F0	RS1	RS0	OV	—	P

CY	PSW.7	Carry Flag
AC	PSW.6	Auxiliary Carry Flag
FO	PSW.5	Flag 0 available to the user for general purpose
RS1	PSW.4	Register Bank selector bit 1
RS0	PSW.3	Register Bank selector bit 0
OV	PSW.2	Overflow Flag
—	PSW.1	User definable flag
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even umber of '1' bits in the accumulator.

With RS1 and RS0 bits we can select the corresponding register bank.

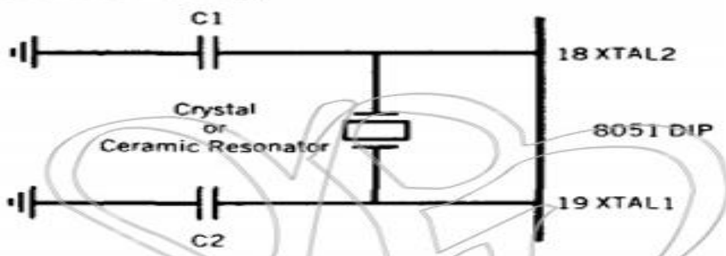
RS1	RS0	Register Bank	Address
0	0	0	00H-07H
0	1	1	08H-0FH
1	0	2	10H-17H
1	1	3	18H-1FH

The 8051 oscillator and clock

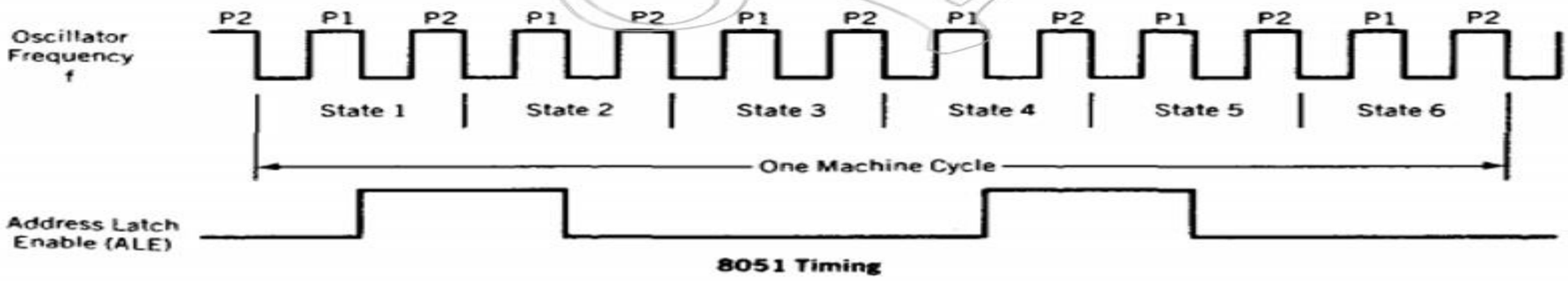
- The 8051 requires an external oscillator circuit. The oscillator circuit usually runs around 12MHz. The crystal generates 12M pulses in one second.
- A machine cycle is minimum amount time must take by simplest machine instruction
- An 8051 machine cycle consists of 12 crystal pulses (clock cycle).
- The first 6 crystal pulses (clock cycle) is used to fetch the Opcode and the second 6 pulses are used to perform the operation on the operands in the ALU.
- This gives an effective machine cycle rate at 1MIPS (Million Instructions Per Second).

Oscillator circuit and timing

Oscillator Circuit and Timing



Crystal or Ceramic Resonator Oscillator Circuit



8051 Timing

Program counter (PC)

- The program counter points to the address of the next instruction to be Executed
- As the CPU fetches the opcode from the program ROM, the program counter is increasing to point to the next instruction.
- The program counter is 16 bits wide
- This means that it can access program addresses 0000 to FFFFH, a total of 64K bytes of code

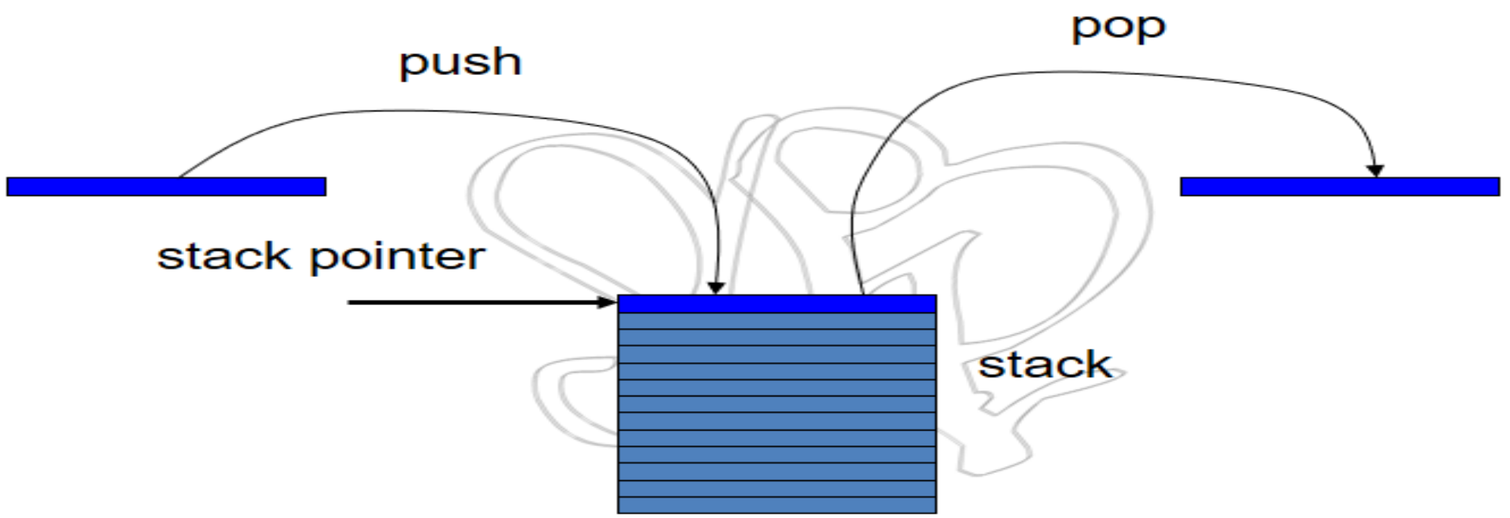
Data pointer (DPTR)

- The data pointer is 16 bit register.
- It is used to hold the address of the data in the memory.
- The DPTR register can be accessed separately as lower eight bit(DPL) and higher eight bit (DPH).
- It can be used as a 16 bit data register or two independent data register.

The stack and The stack pointer (SP)

- The stack is a section of RAM used by the CPU to store information temporarily
- This information could be data or an address
- The register used to access the stack is called the SP (stack pointer) register
- The stack pointer in the 8051 is only 8 bit wide.

Operation of stack



Internal memory

- 128 bytes of RAM.
- Directly addressable range:
  00 to 7F hexadecimal.
- Indirectly addressable range:
  00 to FF hexadecimal.
- Bit addressable space:
  20 to 2F hexadecimal .
- Four register banks:
  00 to 1F hexadecimal.

Internal RAM

The 128 byte internal RAM shown in figure
It is organized into three areas.

1.Working register:
- Thirty-two bytes from address 00h to 1Fh that make up 32 working register organized as Four bank of eight bit each.
- Bits RS0 and RS1 in the PSW determine which bank of register is currently Is use.
- Bank 0 is selected upon reset

2.Bit addressable:
- A bit addressable area of 16 bytes occupies RAM bytes addresses 20h to 2Fh,forming A total of 128 addressable bits.
- An addressable bit may be specified by its bit address of 00h to 7Fh.

3.General purpose:
- A general-purpose RAM area above the bit area,form 30h to 7Fh,addresable as bytes.

External memory

External memory is used in cases when the **internal ROM and RAM memory** Available On chip is **not sufficient**. Two separate are made available by the 16-bit PC and the DPTR and by different control pins for enabling external ROM and RAM chips.

If the **128 bytes of internal RAM is insufficient**, the **external RAM is accessed by the DPTR**. In the 8051 family, **external RAM of upto 64 KB** can be added to any chip.

I/O Ports

-Four 8-bit I/O ports.

- Port 0
- Port 1
- Port 2
- Port 3

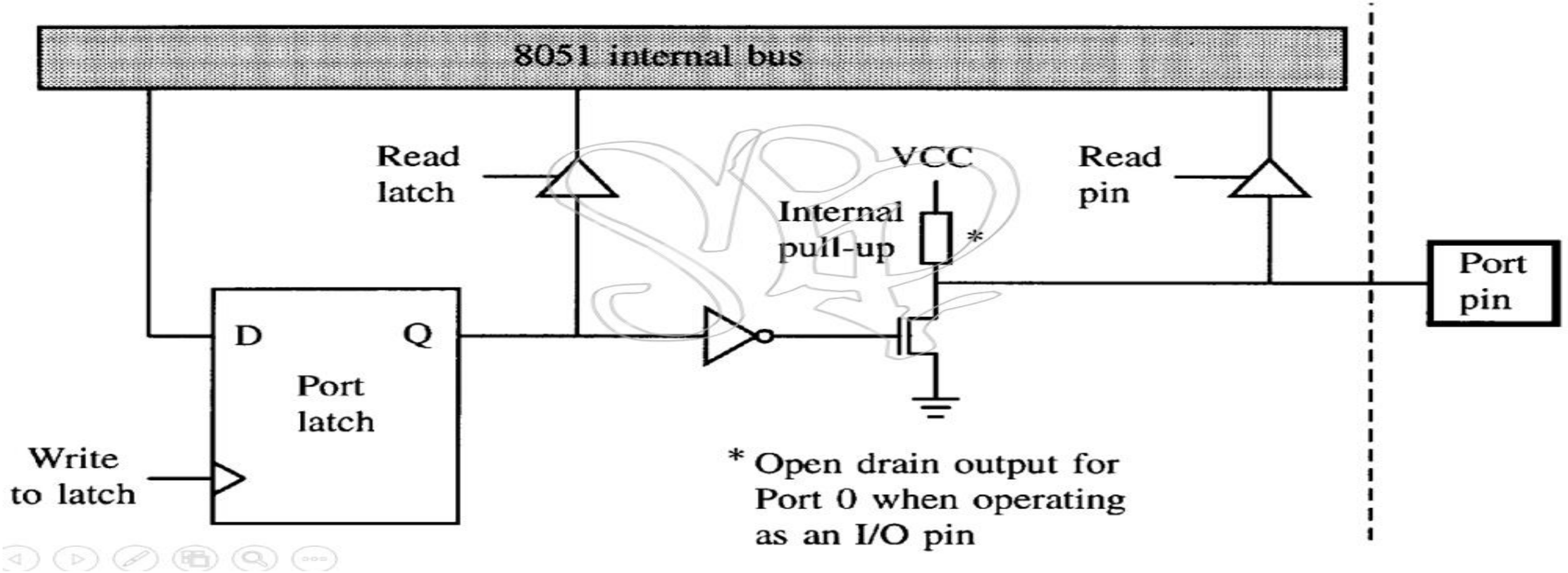
- Most have alternate functions.

- Quasi-bidirectional:

I/O Port structure

- The internal circuitry for the I/O port is shown in the figure
- If you want to read in from a pin, you must first give a logic ‘1’ to the port latch to turn off the FET otherwise the data read in will always be logic ‘0’.
- When you write to the port you are actually writing to the latch e.g. a logic 0 given to the latch will be inverted and turn on the FET which cause the port pin to be connected to Gnd (logic 0).

I/O Port structure Diagram



Interrupt System

- 5 Interrupt Sources (in order of priority):
  1. External Interrupt 0 (IE0)
  2. Timer 0 (TF0)
  3. External Interrupt 1 (iE1)
  4. Timer 1 (TF1)
  5. Serial Port (RI/TI)
- Each interrupt type has a separate vector address.
- Each interrupt type can be programmed to one of two priority levels.
- External interrupts can be programmed for edge or level sensitivity.

THANK YOU