SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

19ECT221 – MICROPROCESSORS AND MICROCONTROLLERS

II YEAR - IV SEM

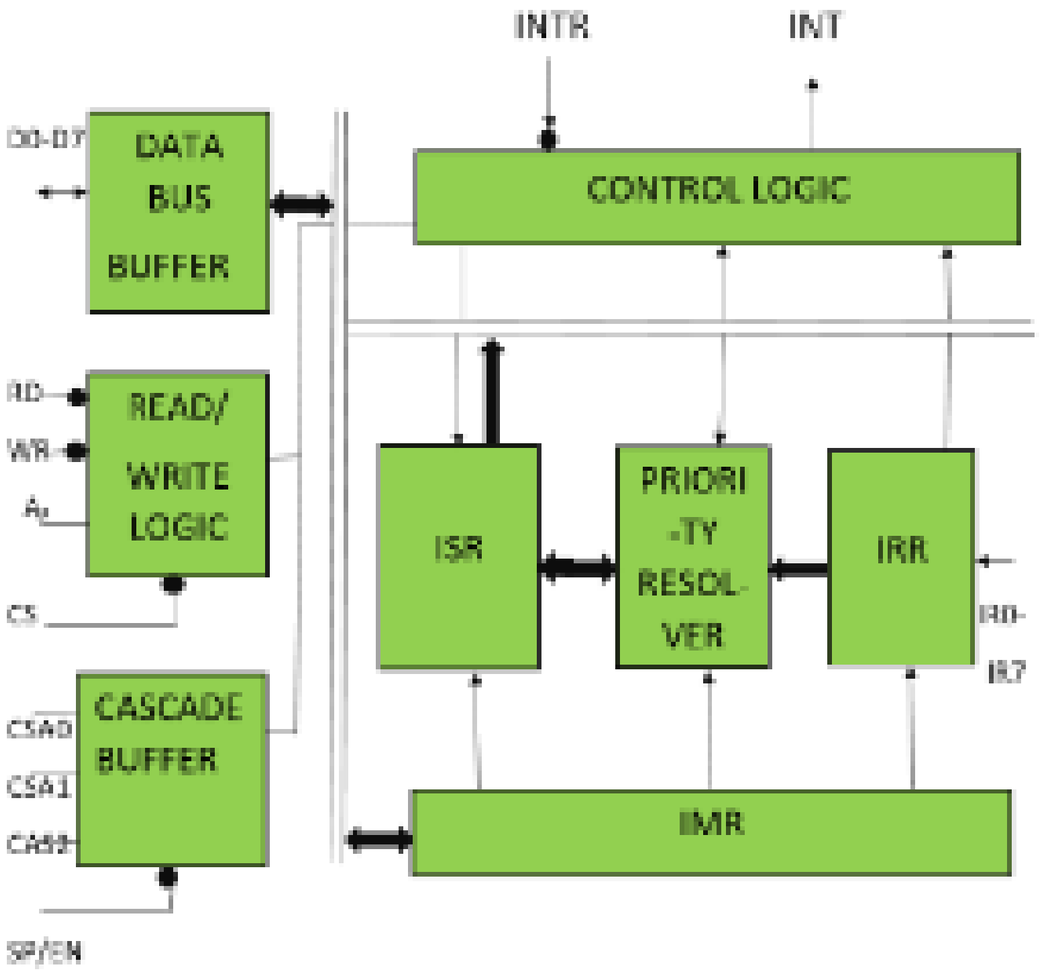
UNIT 2 – 8259 Interrupt Controller

8259- Interrupt Controller

- Intel 8259 is a **Programmable Interrupt Controller (PIC)**.
- There are 5 hardware interrupts and 2 hardware interrupts in Intel 8085 and Intel 8086 microprocessors respectively.
- Intel 8259 is designed for Intel 8085 and Intel 8086 microprocessor.
- It can be programmed either in level triggered or in edge triggered interrupt level.
- We can mask individual bits of interrupt request register.
- We can increase interrupt handling capability upto 64 interrupt level by cascading further 8259 PICs.
- Clock cycle is not required.

Architecture of 8259

$\overline{CS}$	1		28	Vcc
$\overline{WR}$	2		27	A0
$\overline{RD}$	3		26	$\overline{INTA}$
D7	4		25	IR7
D6	5		24	IR6
D5	6		23	IR5
D4	7	8259	22	IR4
D3	8	PIC	21	IR3
D2	9		20	IR2
D1	10		19	IR1
D0	11		18	IR0
CAS0	12		17	INT
CAS1	13		16	$\overline{SP}/\overline{EN}$
Gnd	14		15	CAS2



Features of 8259

➢**Data bus buffer –** mediator between 8259 and 8085/8086 microprocessor by acting as a buffer.

➢ It takes the control word from the 8085 (let say) microprocessor and transfer it to the control logic of 8259 microprocessor.

➢**Read/Write logic –** This block works only when the value of pin CS is low (as this pin is active low). This block is responsible for the flow of data depending upon the inputs of RD and WR. These two pins are active low pins used for read and write operations.

Features of 8259

Control logic –It has pin INTR which is connected with other microprocessor for taking interrupt request and pin INT for giving the output.

If 8259 is enabled, and the other microprocessor Interrupt flag is high then this causes the value of the output INT pin high and 8259 responds.

Interrupt request register (IRR) – It stores all the interrupt level which are requesting for Interrupt services.

Interrupt service register (ISR) – It stores the interrupt level which are currently being executed.

Interrupt mask register (IMR) – It stores the interrupt level which have to be masked by storing the masking bits of the interrupt level.

Features of 8259

Priority resolver – It examines all the three registers and set the priority of interrupts and according to the priority of the interrupts, interrupt with highest priority is set in ISR register.

Also, it reset the interrupt level which is already been serviced in IRR.

Cascade buffer – To increase the Interrupt handling capability, we can further cascade more number of pins by using cascade buffer.

So, during increment of interrupt capability, CSA lines are used to control multiple interrupt structure.

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References

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