SNS COLLEGE OF TECHNOLOGY

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

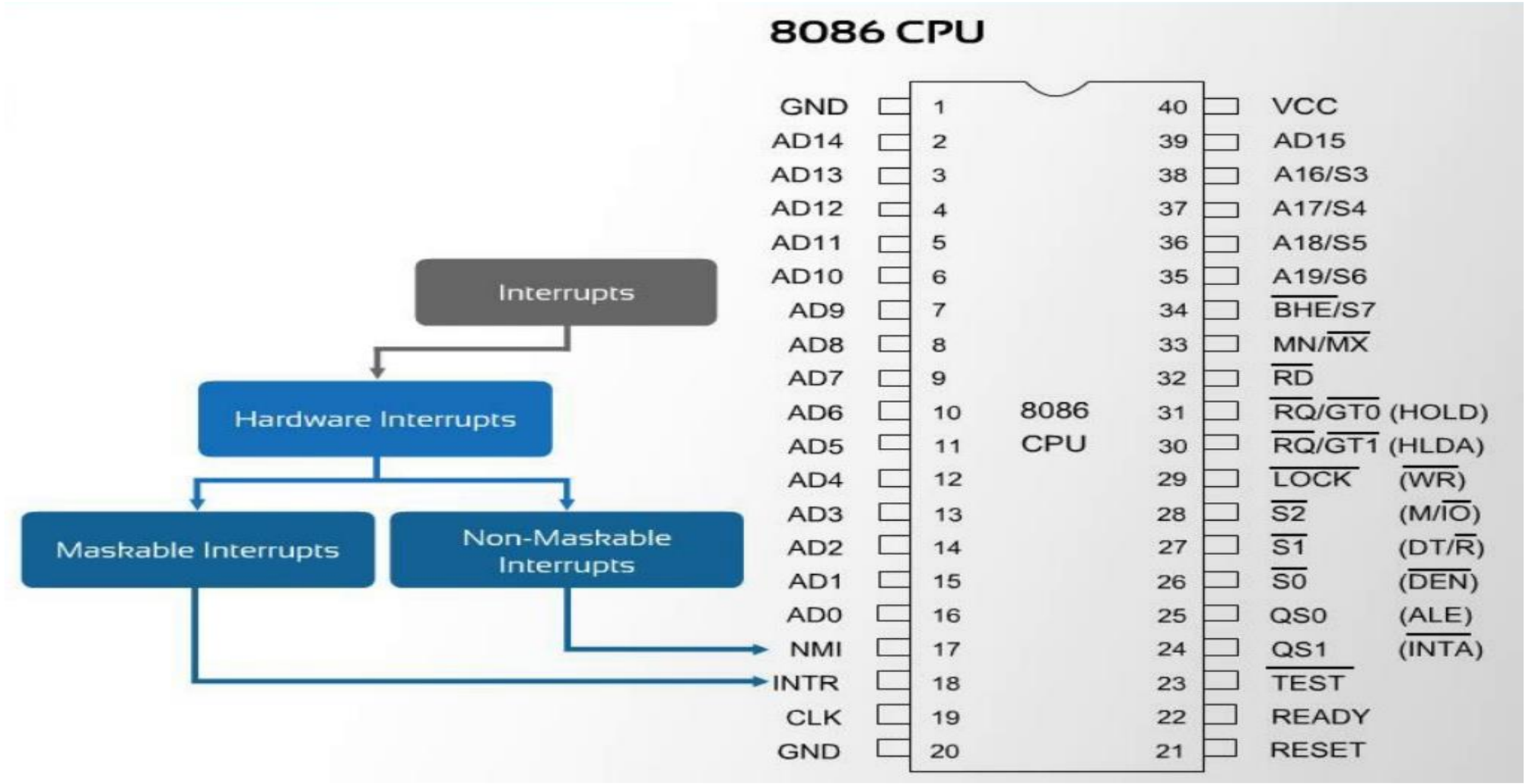
19ITT204 - MICROCONTROLLER AND EMBEDDED SYSTEMS

II YEAR/ IV SEMESTER

UNIT II PERIPHERAL INTERFACING

TOPIC – 8259 interrupt Controller

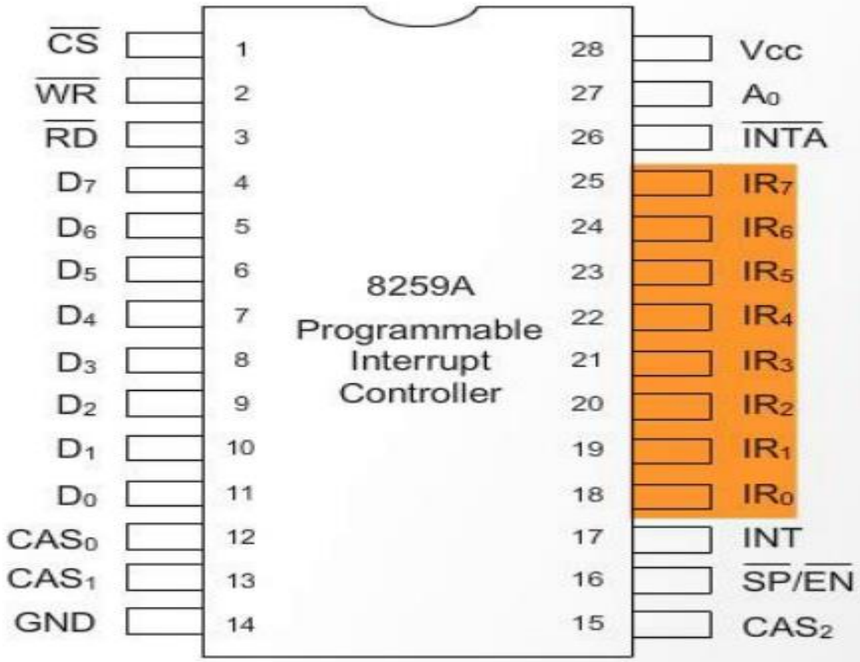
OUTLINE


Interrupts
Hardware Interrupts
Maskable Interrupts
Non-Maskable Interrupts
8086 CPU
GND 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
GND 20
8086 CPU
40 VCC
39 AD15
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
34 BHE/S7
33 MN/MX
32 RD
31 RQ/GT0 (HOLD)
30 RQ/GT1 (HLDA)
29 LOCK (WR)
28 S2 (M/IO)
27 S1 (DT/R)
26 S0 (DEN)
25 QS0 (ALE)
24 QS1 (INTA)
23 TEST
22 READY
21 RESET

8259 Programmable Interrupt Controller (PIC)

1. This IC is designed to simplify the implementation of the interrupt interface in the 8088 and 8086 based microcomputer systems.
2. This device is known as a 'Programmable Interrupt Controller' or PIC.
3. It is manufactured using the NMOS technology and It is available in 28-pin DIP.
4. The operation of the PIC is programmable under software control (Programmable)and it can be configured for a wide variety of applications.
5. 8259A is treated as peripheral in a microcomputer system.
6. 8259A PIC adds eight vectored priority encoded interrupts to the microprocessor.
7. This controller can be expanded without additional hardware to accept up to 64 interrupt request inputs. This expansion required a master 8259A and eight 8259A slaves.
8. Some of its programmable features are:
   - The ability to accept level-triggered or edge-triggered inputs.
   - The ability to be easily cascaded to expand from 8 to 64 interrupt-inputs.
   - Its ability to be configured to implement a wide variety of priority schemes.

8259 PIC



Upto eight Hardware Interrupting devices are supported.

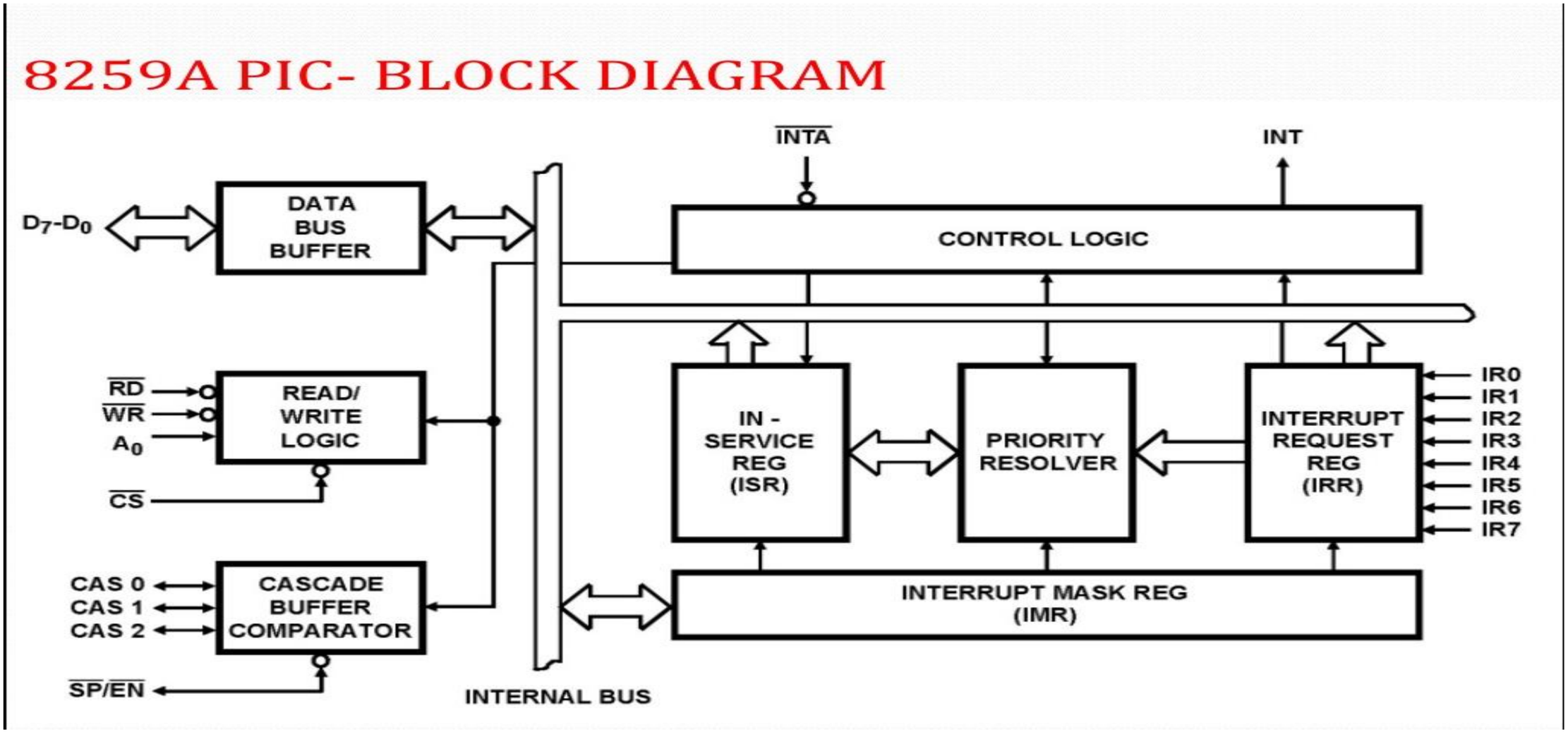
The processor is interrupted whenever the Interrupting device delivers a signal to the 8259.

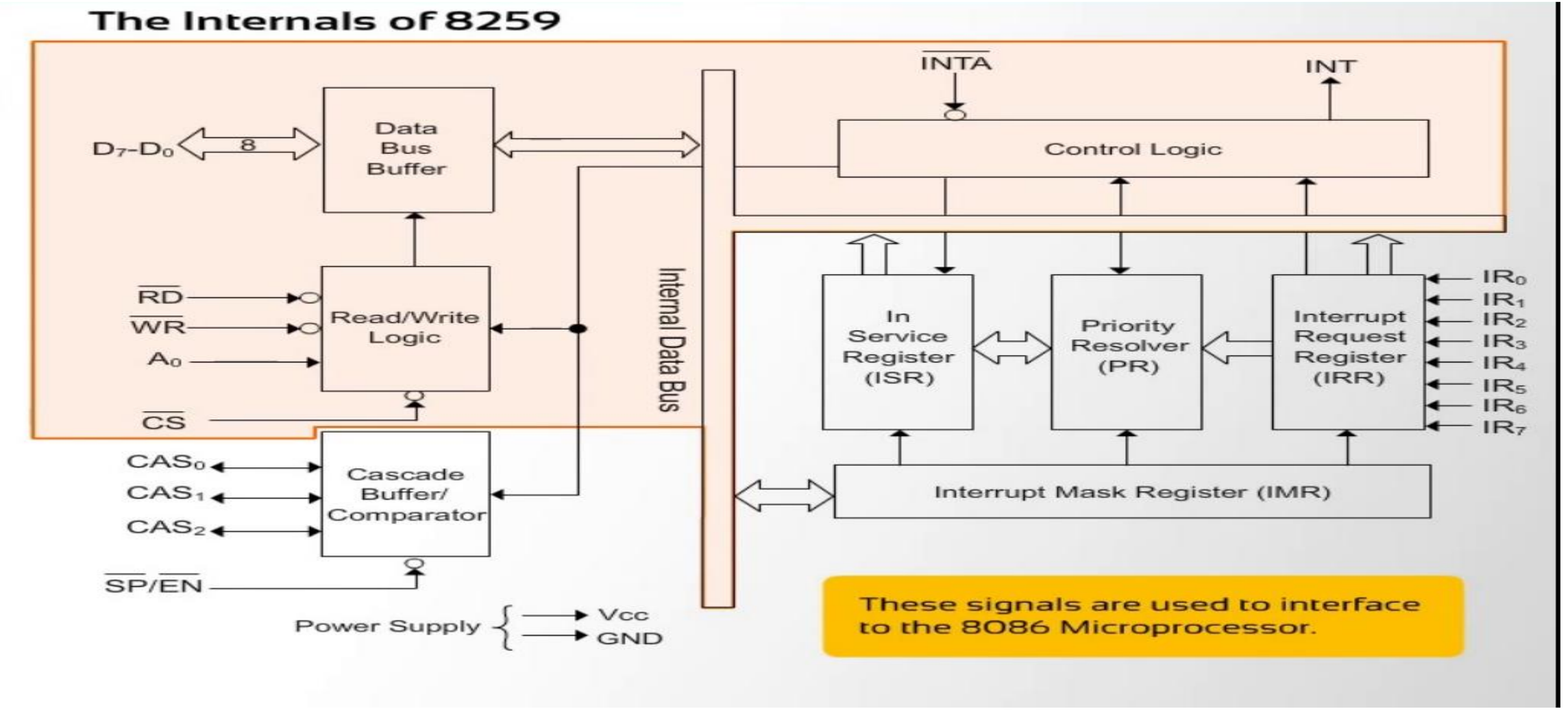
ASSINGMENT OF SIGNALS FOR 8259:

1. **D7- D0** is connected to microprocessor data bus D7-D0 (AD7-AD0).
2. **IR7- IR0**, Interrupt Request inputs are used to request an interrupt and to connect to a slave in a system with multiple 8259As.
3. **$\overline{WR}$** - the write input connects to write strobe signal of microprocessor.
4. **$\overline{RD}$** - the read input connects to the IORC signal.
5. **INT** - the interrupt output connects to the INTR pin on the microprocessor from the master, and is connected to a master IR pin on a slave.
6. **$\overline{INTA}$** - the interrupt acknowledge is an input that connects to the INTA signal on the system. In a system with a master and slaves, only the master INTA signal is connected.
7. **A0** - this address input selects different command words within the 8259A.
8. **$\overline{CS}$** - chip select enables the 8259A for programming and control.
9. **$\overline{SP}/\overline{EN}$** - Slave Program/Enable Buffer is a dual-function pin.

- When the 8259A is in buffered mode, this pin is an output that controls the data bus transceivers in a large microprocessor-based system.
- When the 8259A is not in buffered mode, this pin programs the device as a master (1) or a slave (0).
- CAS2-CAS0, the cascade lines are used as outputs from the master to the slaves for cascading multiple 8259As in a system.

8259A PIC- BLOCK DIAGRAM




The Internals of 8259
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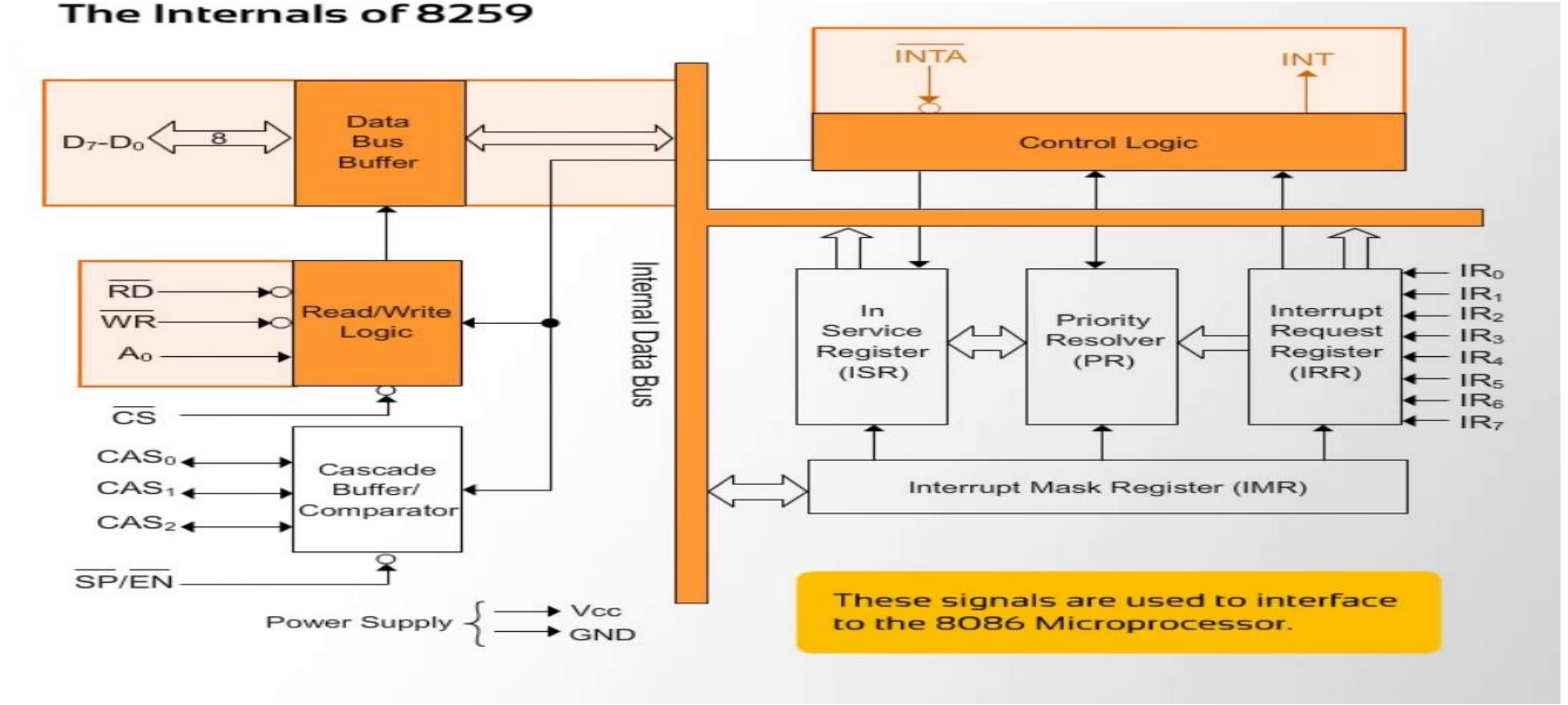
INT
D7-D0
8
Data Bus Buffer
Control Logic
RD
WR
A0
Read/Write Logic
Internal Data Bus
In Service Register (ISR)
Priority Resolver (PR)
Interrupt Request Register (IRR)
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
CS
CAS0
CAS1
CAS2
Cascade Buffer/ Comparator
Interrupt Mask Register (IMR)
SP/EN
Power Supply
Vcc
GND
These signals are used to interface to the 8086 Microprocessor.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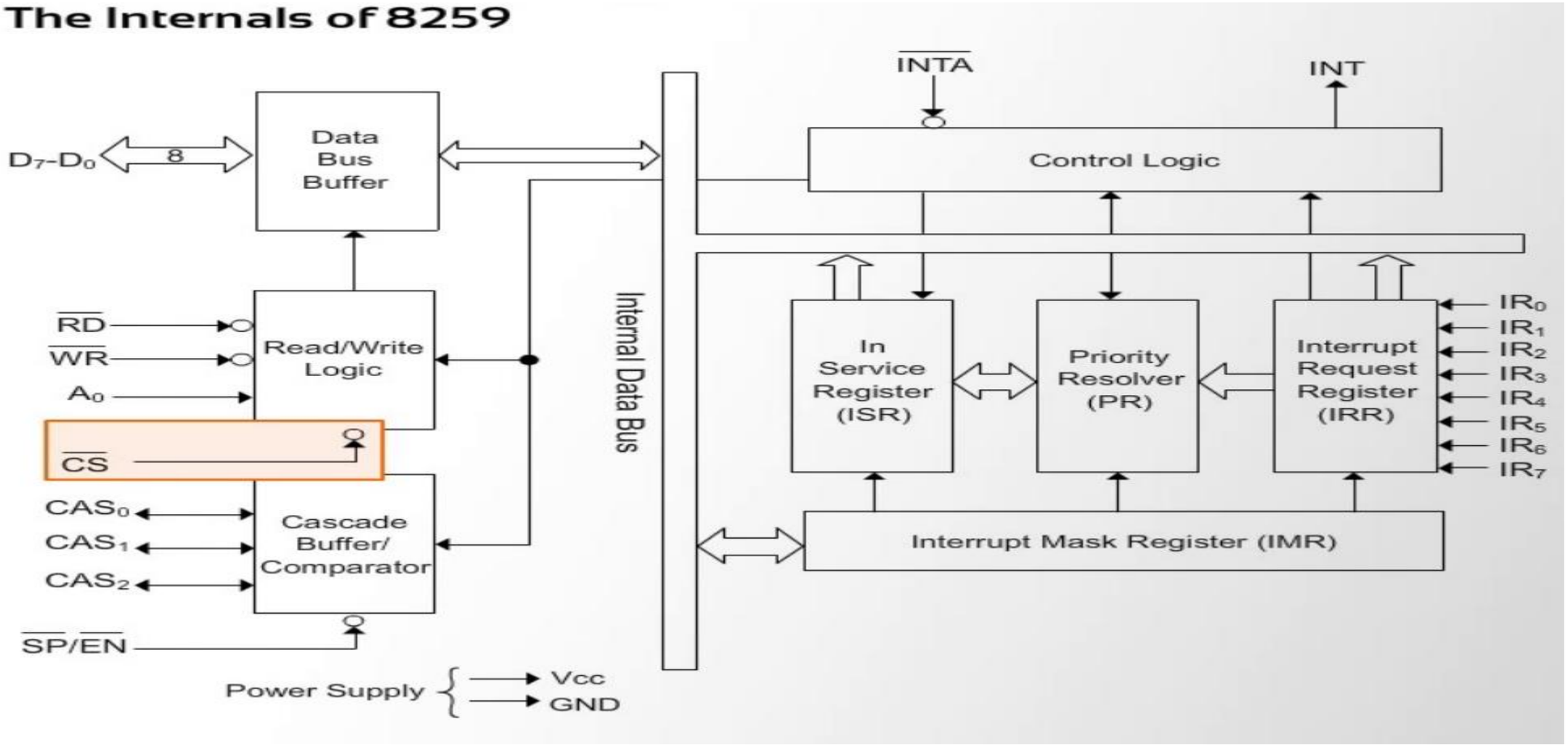
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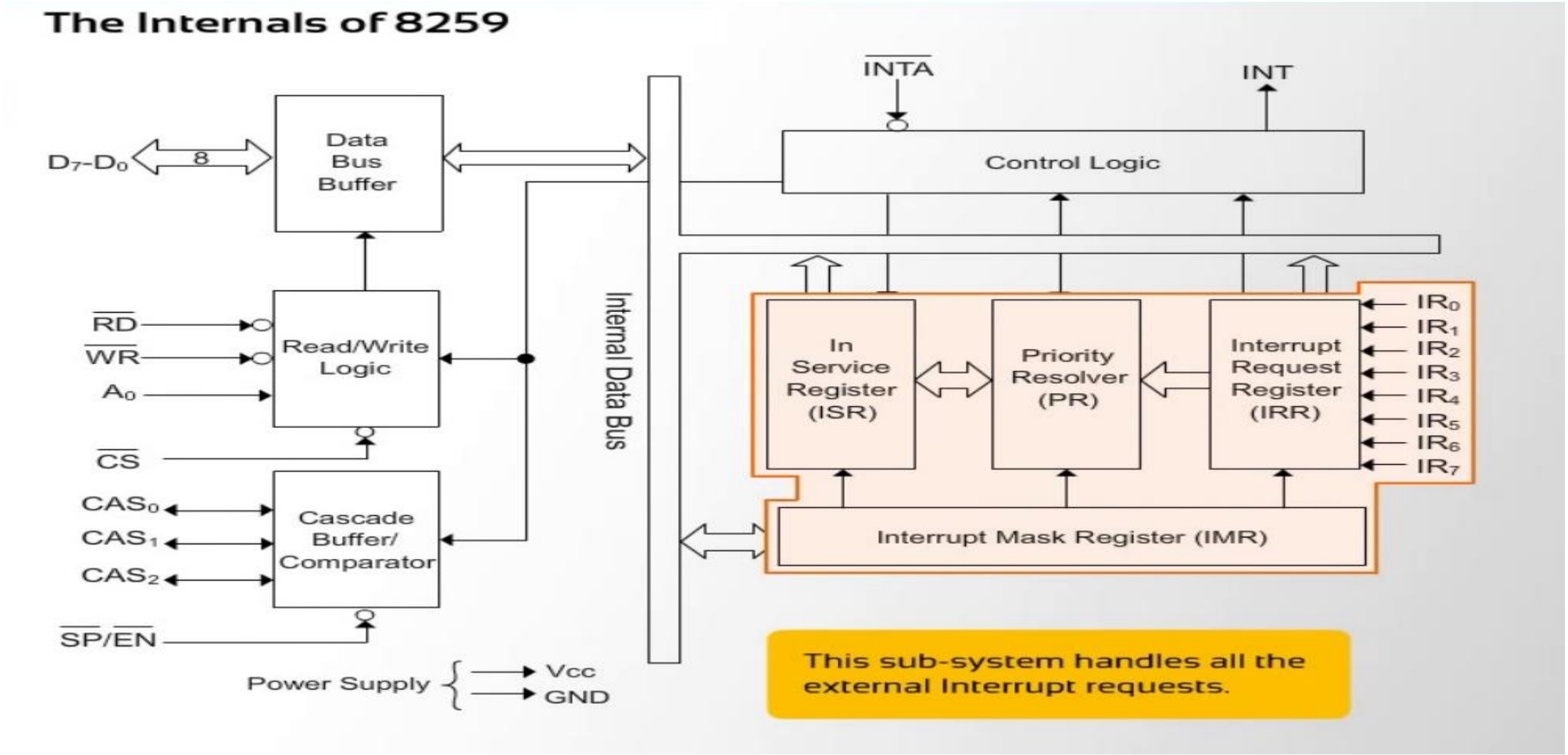
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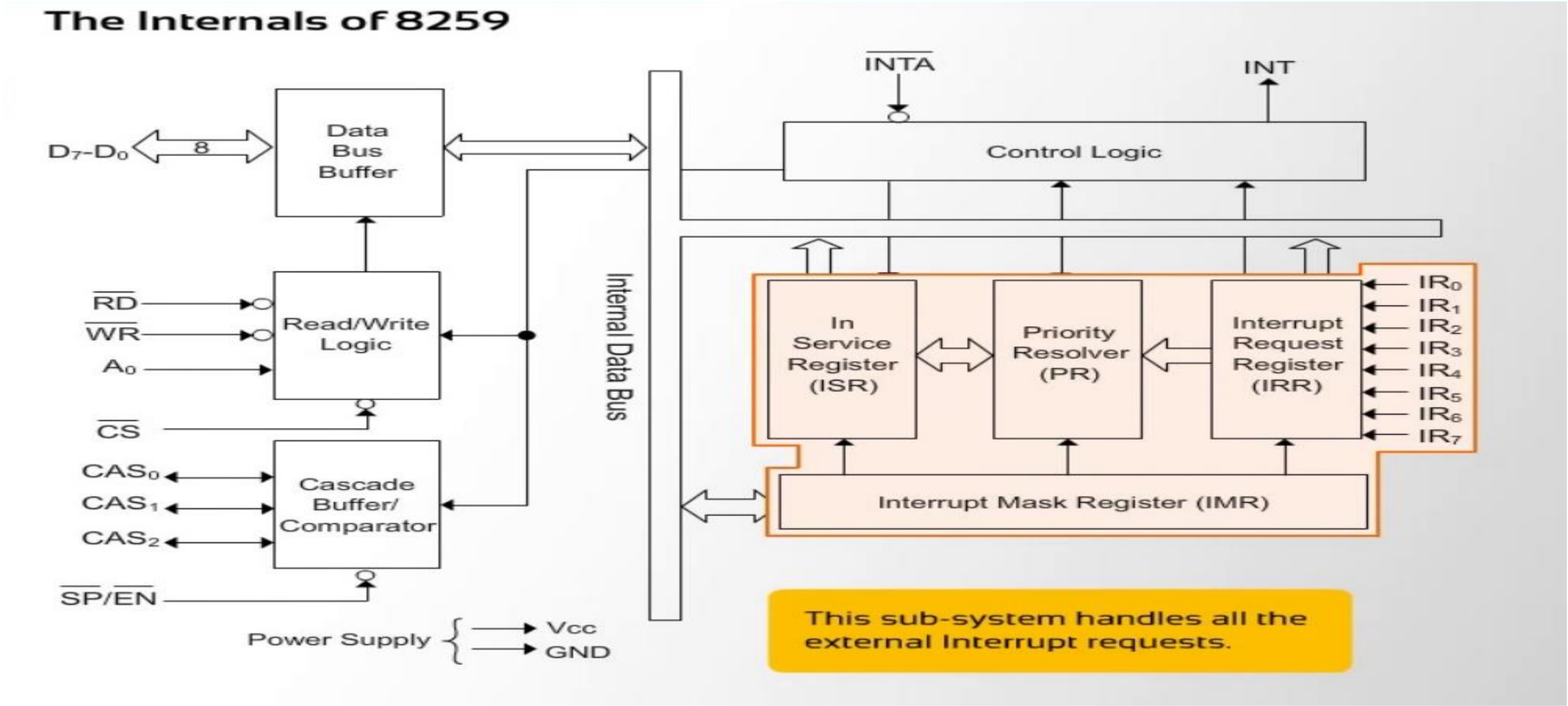
This sub-system handles all the external Interrupt requests.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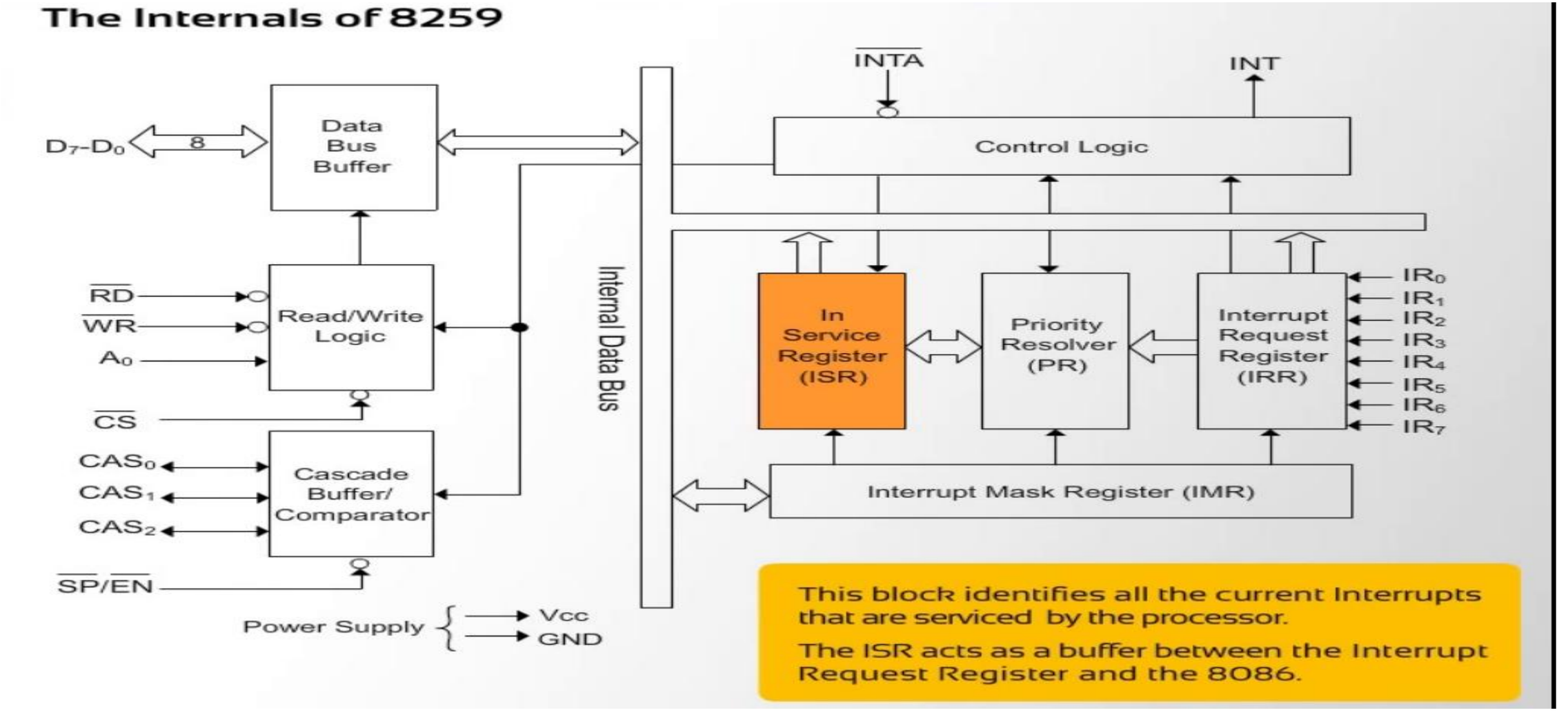
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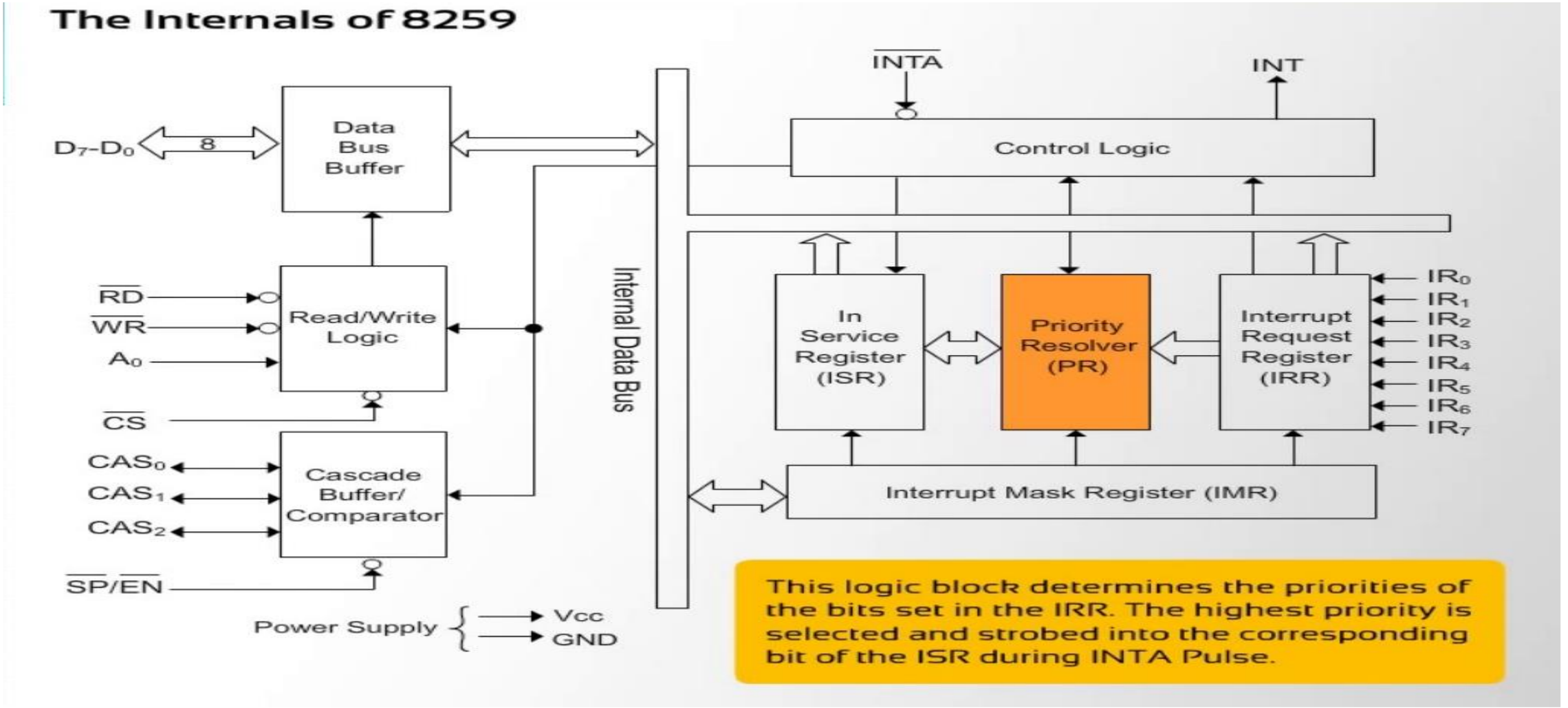
This block identifies all the current Interrupts that are serviced by the processor.
The ISR acts as a buffer between the Interrupt Request Register and the 8086.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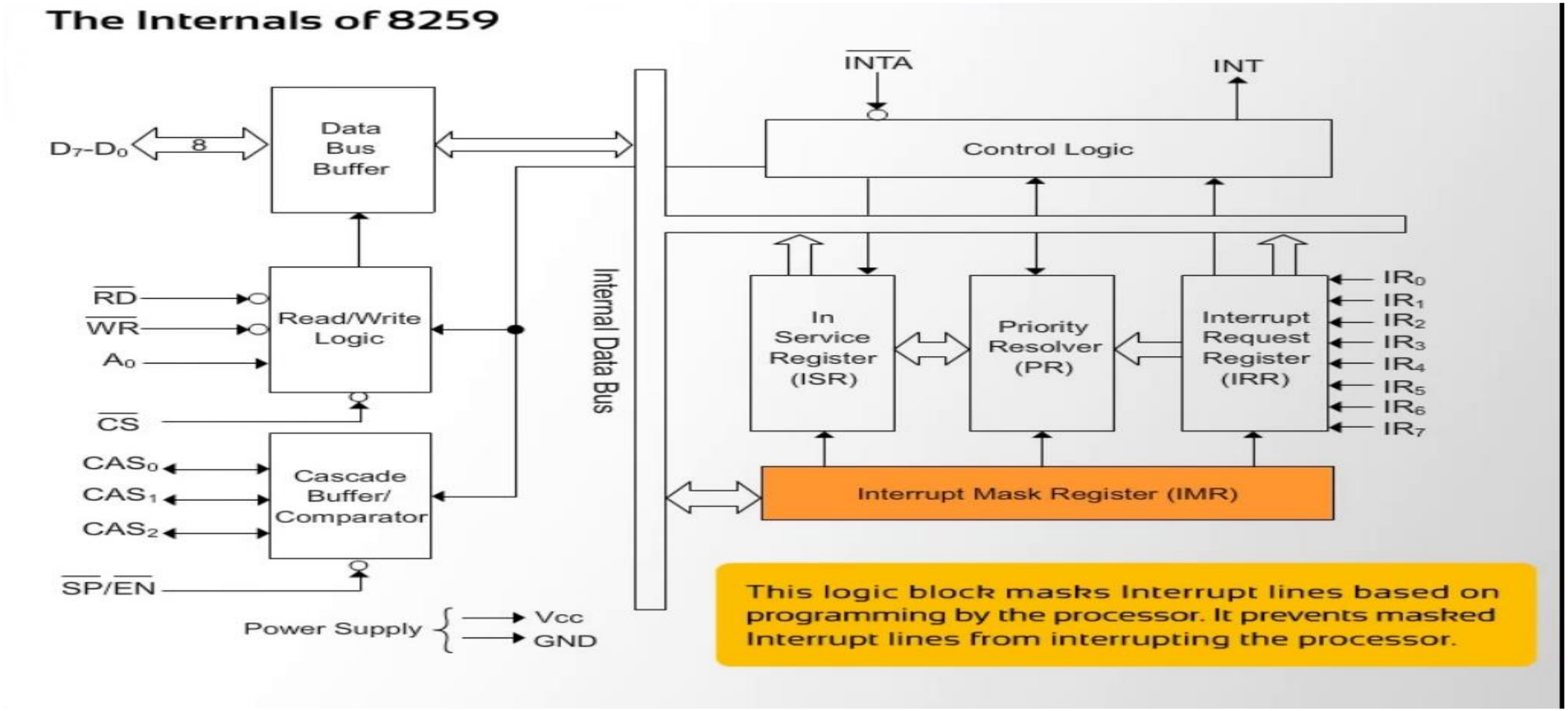
This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during INTA Pulse.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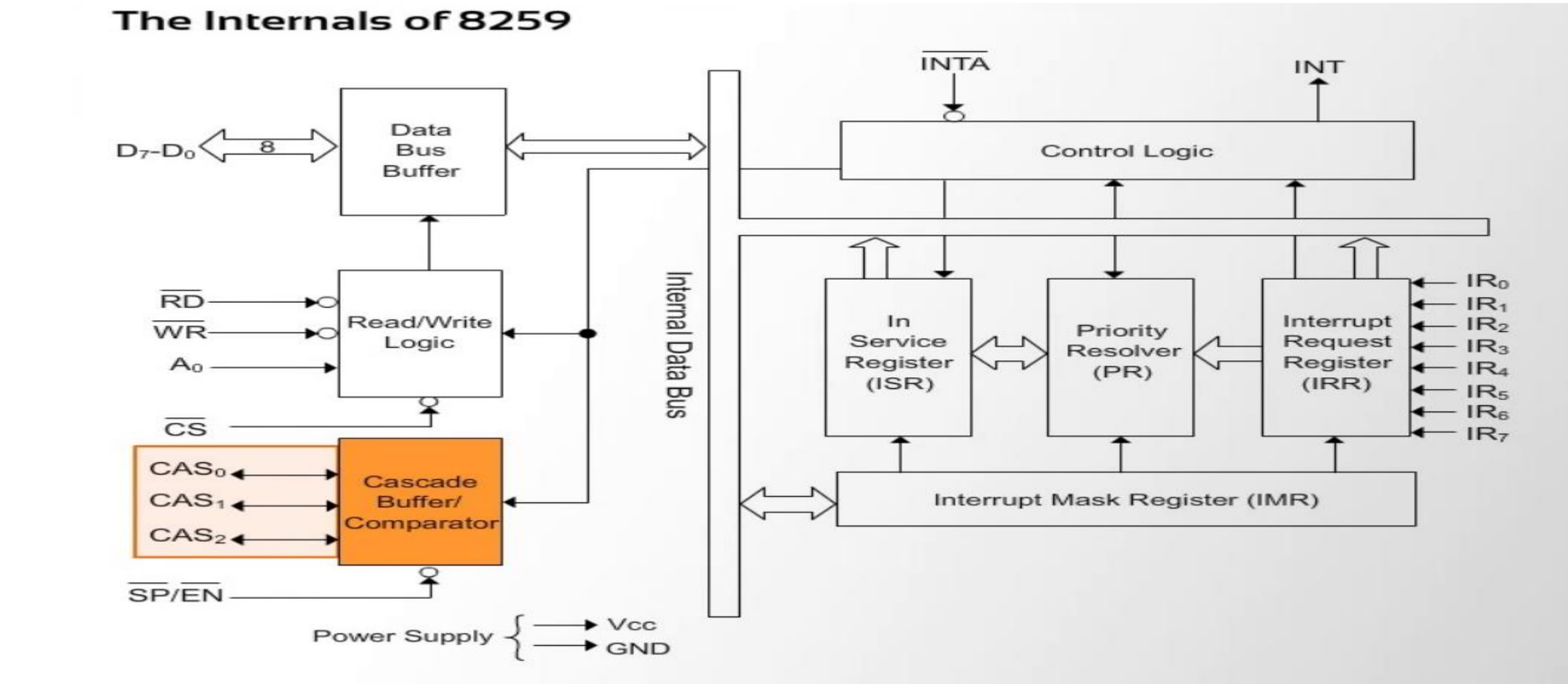
This logic block masks Interrupt lines based on programming by the processor. It prevents masked Interrupt lines from interrupting the processor.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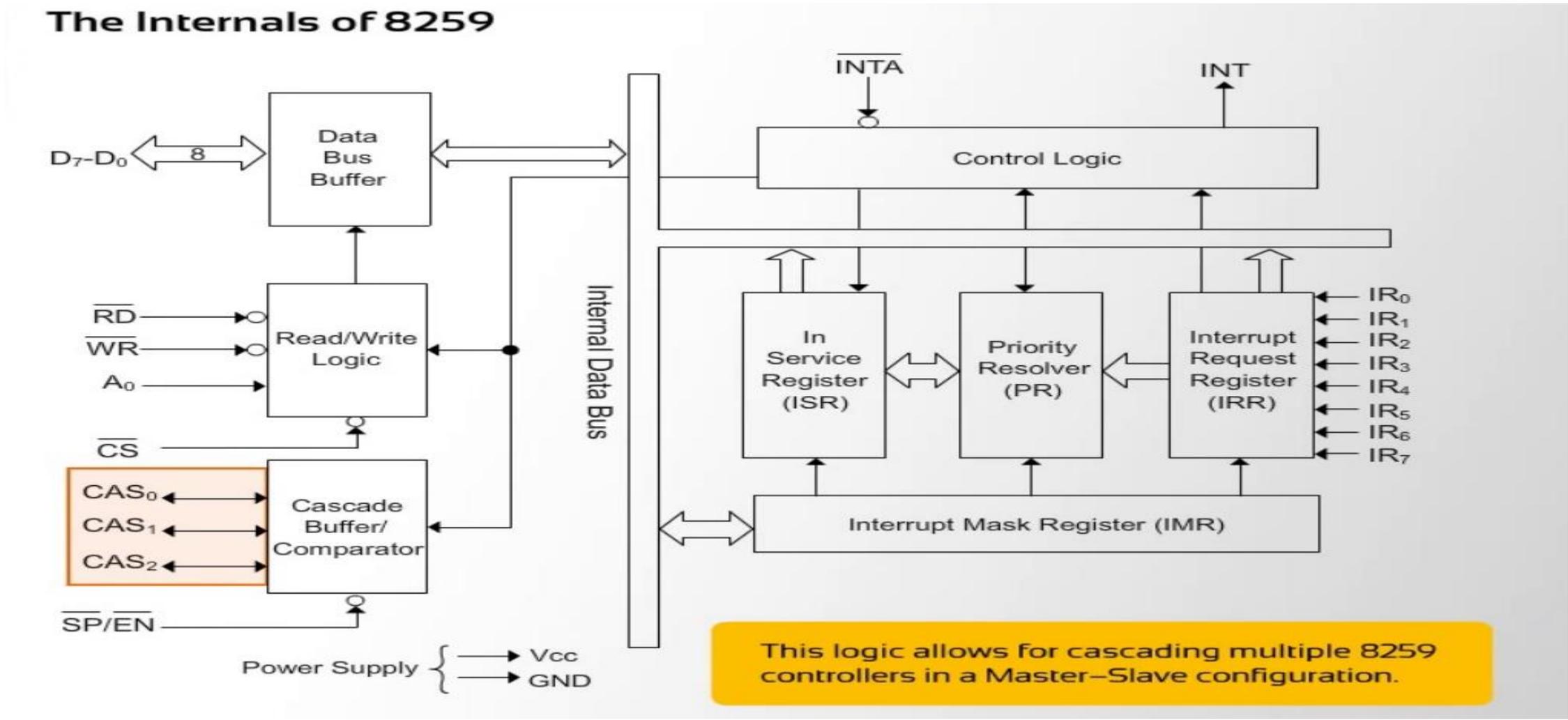
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This logic allows for cascading multiple 8259 controllers in a Master–Slave configuration.

THANK YOU