SNS COLLEGE OF TECHNOLOGY

An Autonomous Institution

Coimbatore-35

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ITT204 - MICROCONTROLLER AND EMBEDDED SYSTEMS

II YEAR/ IV SEMESTER

UNIT II PERIPHERAL INTERFACING

TOPIC – 8251 USART

OUTLINE

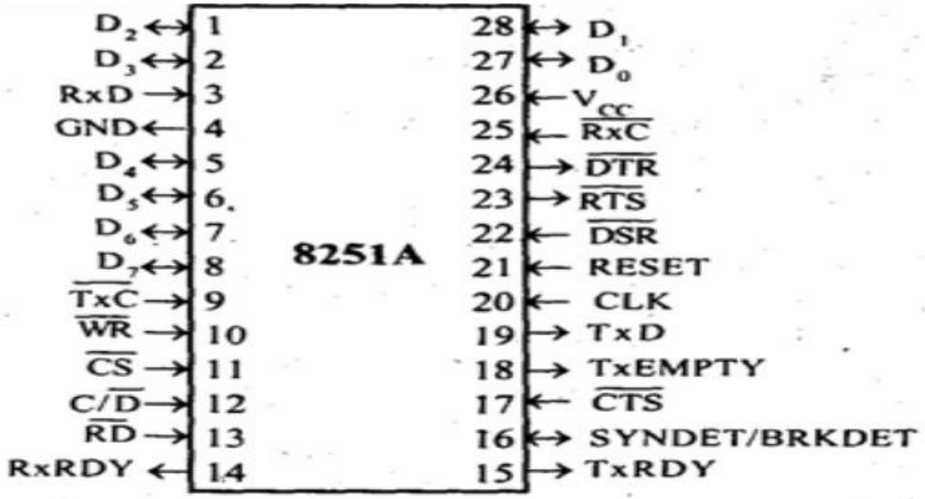
35

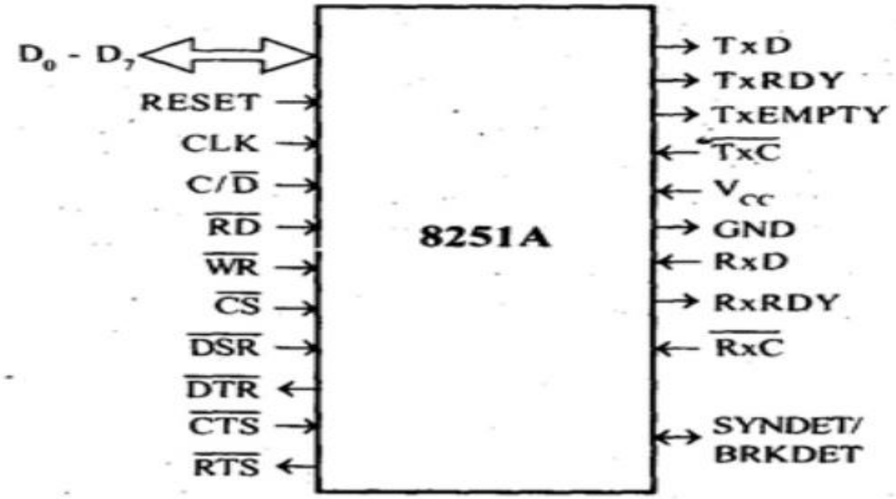
Serial communication interface

INTEL 8251 USART

UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART)

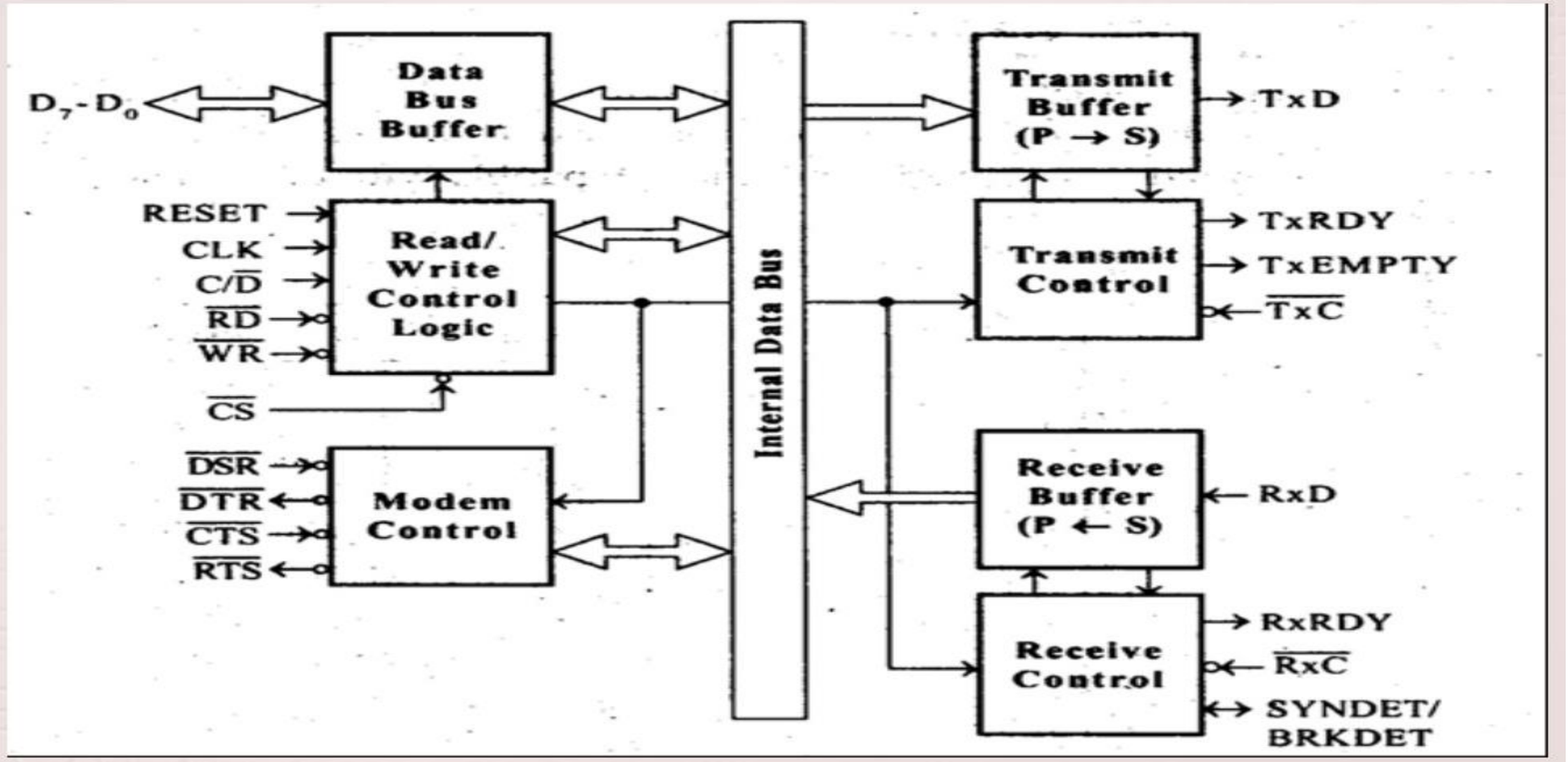
- Programmable chip designed for synchronous and asynchronous serial data transmission
- 28 pin DIP
- Coverts the parallel data into a serial stream of bits suitable for **serial transmission**.
- Receives a serial stream of bits and convert it into parallel data bytes to be read by a microprocessor.





Pin	Description
D_0-D_7	Parallel data
C/$\overline{D}$	Control register or Data buffer select
$\overline{RD}$	Read control
$\overline{WR}$	Write control
$\overline{CS}$	Chip Select
CLK	Clock pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready
TxRDY	Transmitter Ready
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET/ BRKDET	Synchronous Detect / Break Detect
$\overline{RTS}$	Request To Send Data
$\overline{CTS}$	Clear To Send Data
TxEMPTY	Transmitter Empty
V_{CC}	Supply (+5V)
GND	Ground (0 V)

BLOCK DIAGRAM



Five Sections

- **Read/Write Control Logic**
  - Interfaces the chip with MPU
  - Determine the functions according to the control word
  - Monitors data flow
- **Transmitter**
  - Converts parallel word received from MPU into serial bits
  - Transmits serial bits over TXD line to a peripheral.
- **Receiver**
  - Receives serial bits from peripheral
  - Converts serial bits into parallel word
  - Transfers the parallel word to the MPU
- **Data Bus Buffer- 8 bit Bidirectional bus.**
- **Modem Controller**
  - Used to establish data communication modems over telephone line

Input Signals

- $\overline{CS}$ – Chip Select
  - When this signal goes **low**, 8251 is selected by MPU for communication
- C/$\overline{D}$ – Control/Data
  - When this signal is **high**, the **control register** or status register is addressed
  - When it is **low**, the **data buffer** is addressed
  - Control and Status register is differentiated by $\overline{WR}$ and $\overline{RD}$ signals, respectively

- $\overline{WR}$ – Write
  - writes in the control register or sends outputs to the data buffer.
  - This connected to IOW or MEMW
- $\overline{RD}$ – Read
  - Either reads a status from status register or accepts data from the data buffer
  - This is connected to either IOR or MEMR
- RESET - Reset
- CLK - Clock
  - Connected to system clock
  - Necessary for communication with microprocessor.

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	Function
0	1	1	0	MPU writes instruction in the control register
0	1	0	1	MPU reads status from the status register
0	0	1	0	MPU outputs the data to the Data Buffer
0	0	0	1	MPU accepts data from the Data Buffer
1	X	X	X	USART is not Selected

- Control Register
  - 16-bit register
  - This register can be accessed an output port when the C/D pin is high
- Status Register
  - Checks ready status of a peripheral
- Data Buffer

Transmitter Section

- Accepts parallel data and converts it into serial data
- Two registers
  - Buffer Register
    - To hold eight bits
  - Output Register
    - Converts eight bits into a stream of serial bits
  - Transmits data on TxD pin with appropriate framing bits(Start and Stop)

Signals Associated with Transmitter Section

- TxD – Transmit Data
  - Serial bits are transmitted on this line
- TxC – Transmitter Clock
  - Controls the rate at which bits are transmitted
- TxRDY – Transmitter Ready
  - Can be used either to interrupt the MPU or indicate the status
- TxE – Transmitter Empty
  - Logic 1 on this line indicate that the output register is empty

Receiver Section

- Accepts serial data from peripheral and converts it into parallel data
- The section has two registers
  - Input Register
  - Buffer Register

Signals Associated with Receiver Section

- RxD – Receive Data
  - Bits are received serially on this line and converted into parallel byte in the receiver input
- RxC – Receiver Clock
- RxRDY – Receiver Ready
  - It goes high when the USART has a character in the buffer register and is ready to transfer it to the MPU

Signals Associated with Modem Control

- DSR- Data Set Ready
  - Normally used to check if the Data Set is ready when communicating with a modem
- DTR – Data Terminal Ready
  - device is ready to accept data when the 8251 is communicating with a modem.
- RTS – Request to send Data
  - the receiver is ready to receive a data byte from modem
- CTS – Clear to Send

Control words

There are two types of control word.

1. Mode instruction (setting of function)

2. Command (setting of operation)

1) Mode Instruction

Mode instruction is used for setting the function of the 8251. Mode instruction will be in "wait for write" at either internal reset or external reset. That is, the writing of a control word after resetting will be recognized as a "mode instruction."

Items set by mode instruction are as follows:

- Synchronous/asynchronous mode
- Stop bit length (asynchronous mode)
- Character length
- Parity bit
- Baud rate factor (asynchronous mode)

2) Command

Command is used for setting the operation of the 8251. It is possible to write a command whenever necessary after writing a mode instruction and sync characters.

Items to be set by command are as follows:

- Transmit Enable/Disable
- Receive Enable/Disable
- DTR, RTS Output of data.
- Resetting of error flag.
- Sending to break characters
- Internal resetting
- Hunt mode (synchronous mode)

THANK YOU