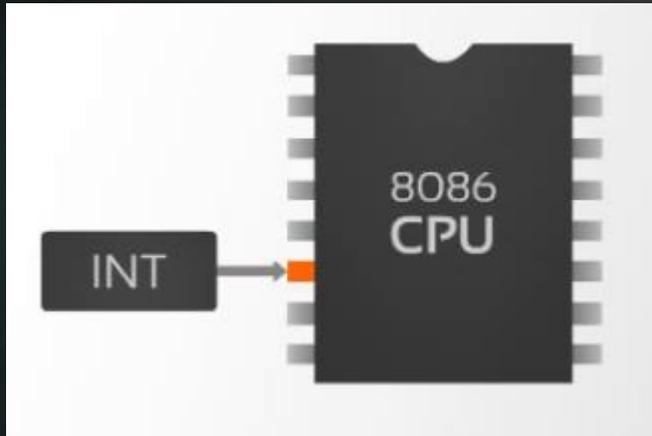




WELCOME

Presented
By
RAJA S
APECE

8086 Microprocessor Interrupts



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Introduction

- The meaning of ‘interrupts’ is to break the sequence of operation.
- While the Microprocessor is executing a program, an ‘interrupt’ breaks the normal sequence of execution of instructions, diverts its execution to some other program called Interrupt Service Routine (ISR).

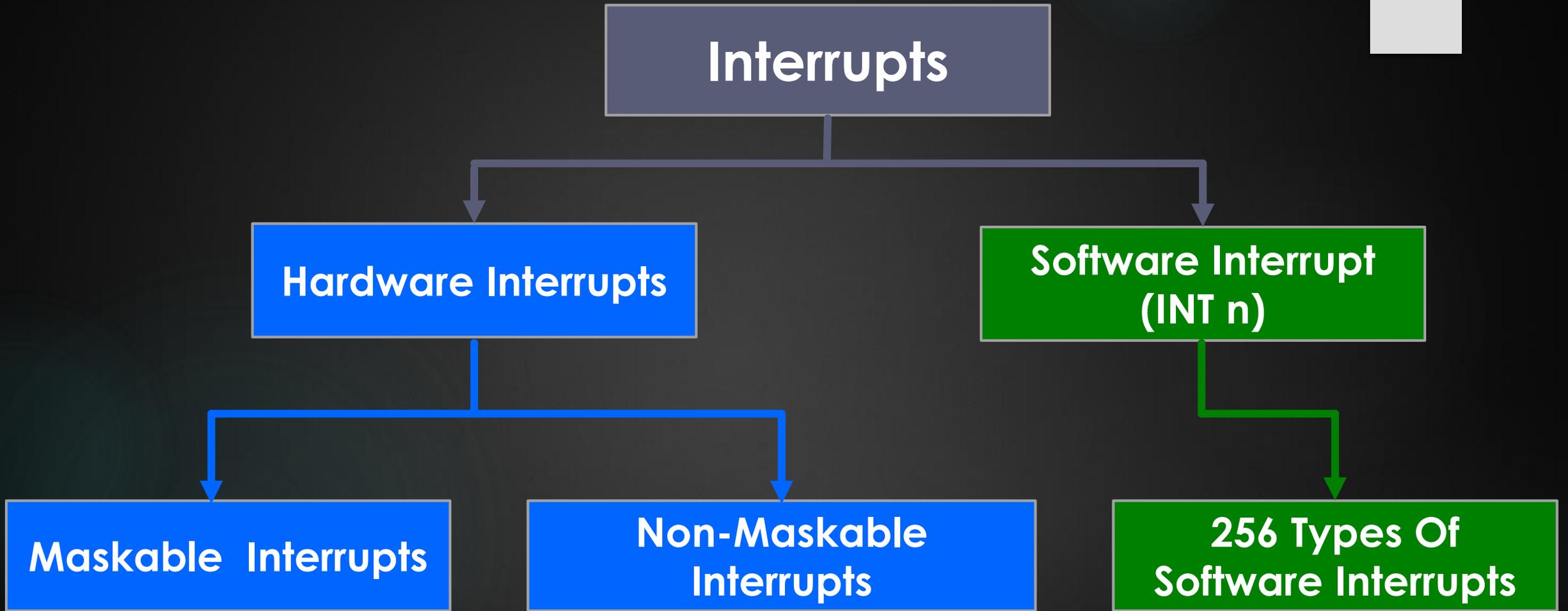
After executing , control returns the back again to the main program.

Interrupt

- Keeping moving until interrupted by the sensor .
- Interrupt received then do pre-defined operation.
- After finishing the interrupt service return to normal operation i.e keep moving forward again.

The processor can be interrupted in the following ways

- i) by an external signal generated by a peripheral,**
- ii) by an internal signal generated by a special instruction in the program,**
- iii) by an internal signal generated due to an exceptional condition which occurs while executing an instruction.**



Hardware Interrupts

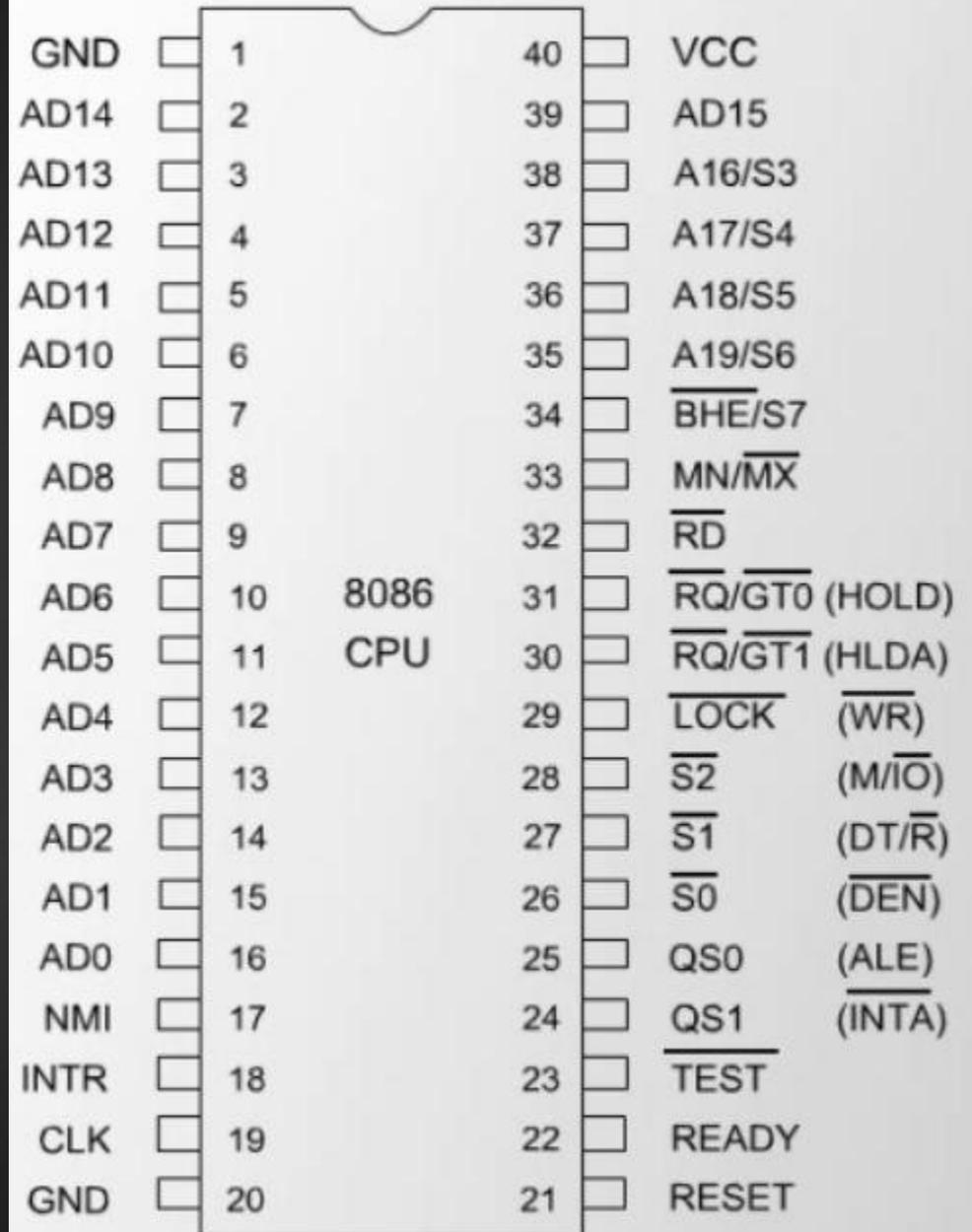
The interrupts initiated by external hardware by sending an appropriate signal to the interrupt pin of the processor is called hardware interrupt. The 8086 processor has two interrupt pins INTR and NMI. The interrupts initiated by applying appropriate signal to these pins are called hardware interrupts of 8086.

Interrupts

Hardware Interrupts

Maskable Interrupts

Non-Maskable Interrupts

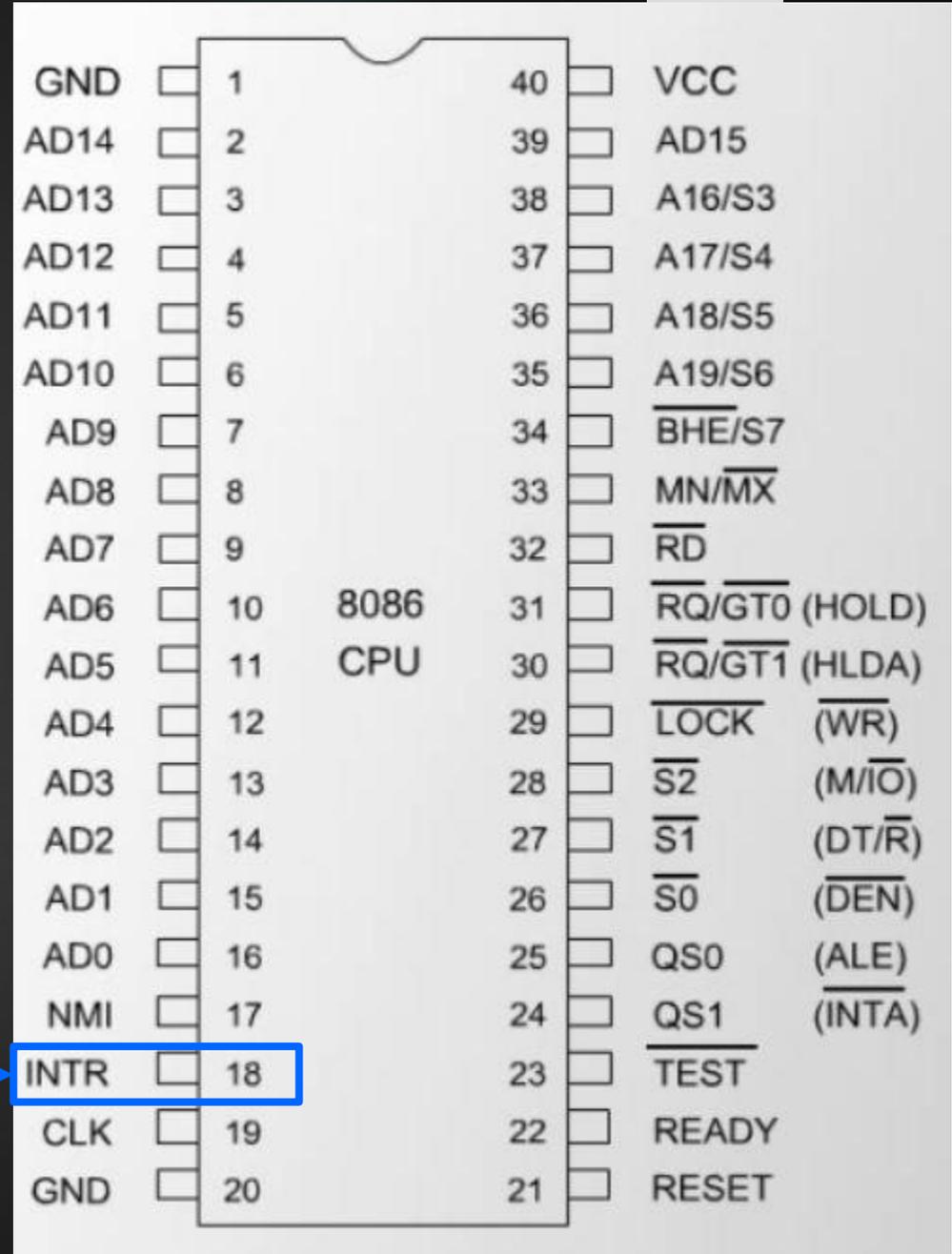


Interrupts

Hardware Interrupts

Maskable Interrupts

Non-Maskable Interrupts

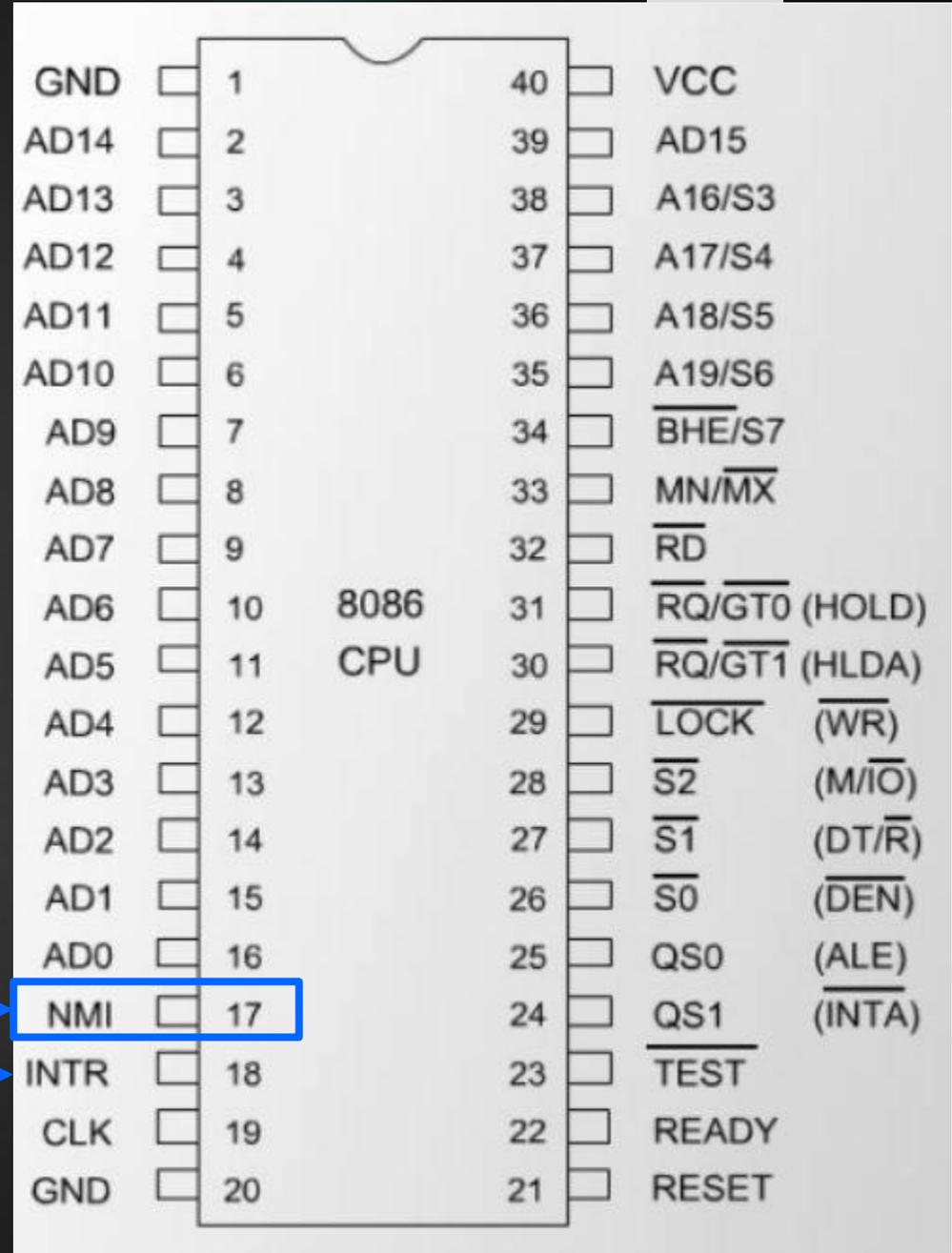


Interrupts

Hardware Interrupts

Maskable Interrupts

Non-Maskable Interrupts



Hardware Interrupts

Used to handle external hardware peripherals , such as key boards , mouse , hard disks , floppy disks , DVD drivers, and printers.



key boards



mouse



hard disks



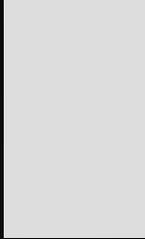
floppy disks



DVD drivers

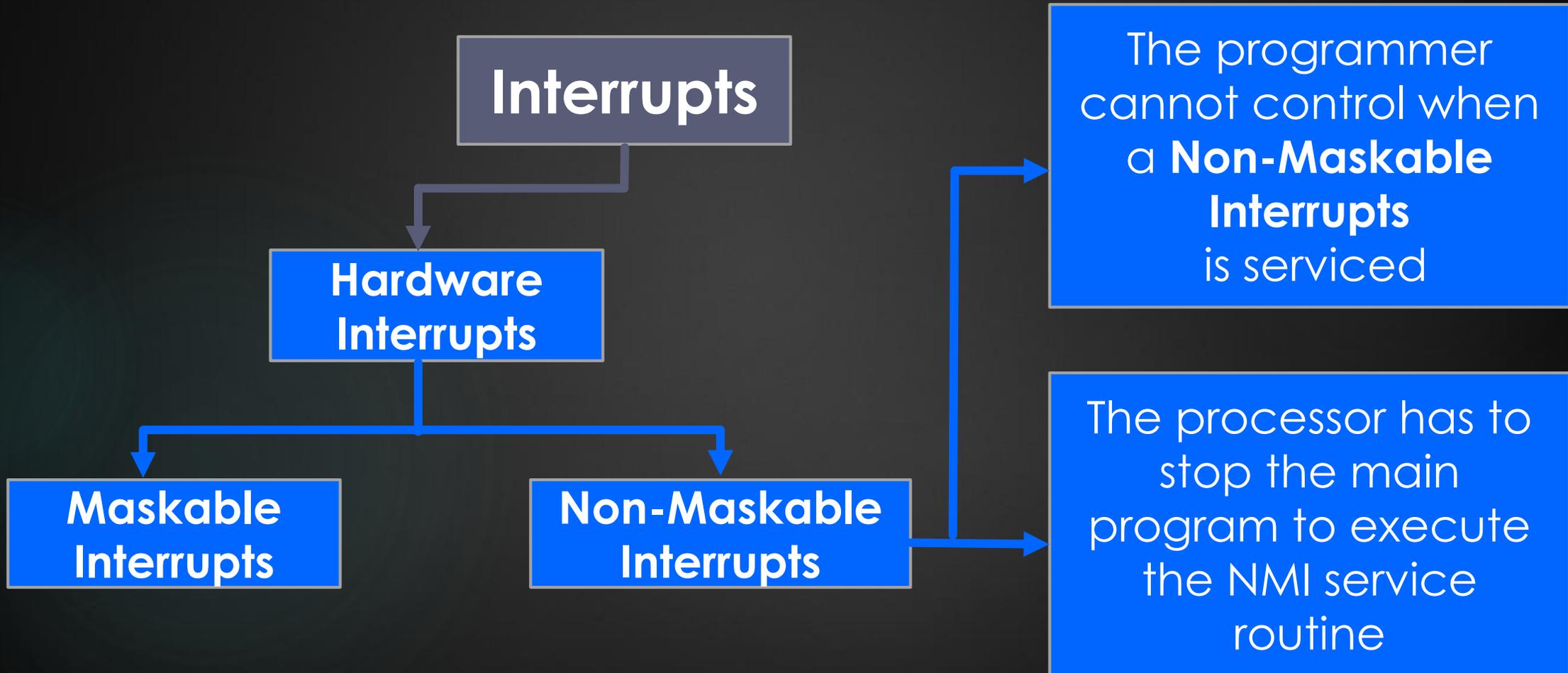
Maskable & Non-Maskable Interrupts

The processor has the facility for accepting or rejecting hardware interrupts. Programming the processor to reject an interrupt is referred to as masking or disabling and programming the processor to accept an interrupt is referred to as unmasking or enabling. In 8086 the interrupt flag (IF) can be set to one to unmask or enable all hardware interrupts and IF is cleared to zero to mask or disable a hardware interrupts except NMI. The interrupts whose request can be either accepted or rejected by the processor are called maskable interrupts.

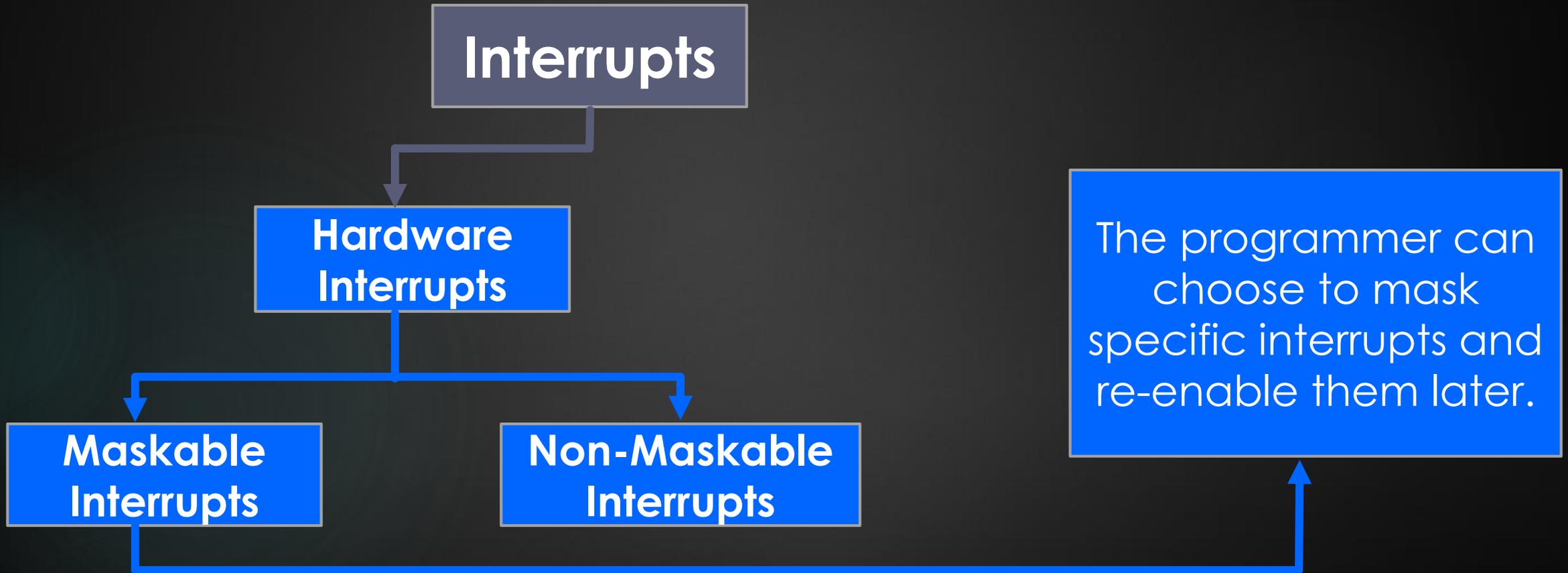


The interrupts whose request has to be definitely accepted (or cannot be rejected) by the processor are called non-maskable interrupts. Whenever a request is made by non-maskable interrupt, the processor has to definitely accept that request and service that interrupt by suspending its current program and executing an ISR. In 8086 processor all the hardware interrupts initiated through INTR pin are maskable by clearing interrupt flag (IF). The interrupt initiated through NMI pin and all software interrupts are non-maskable.

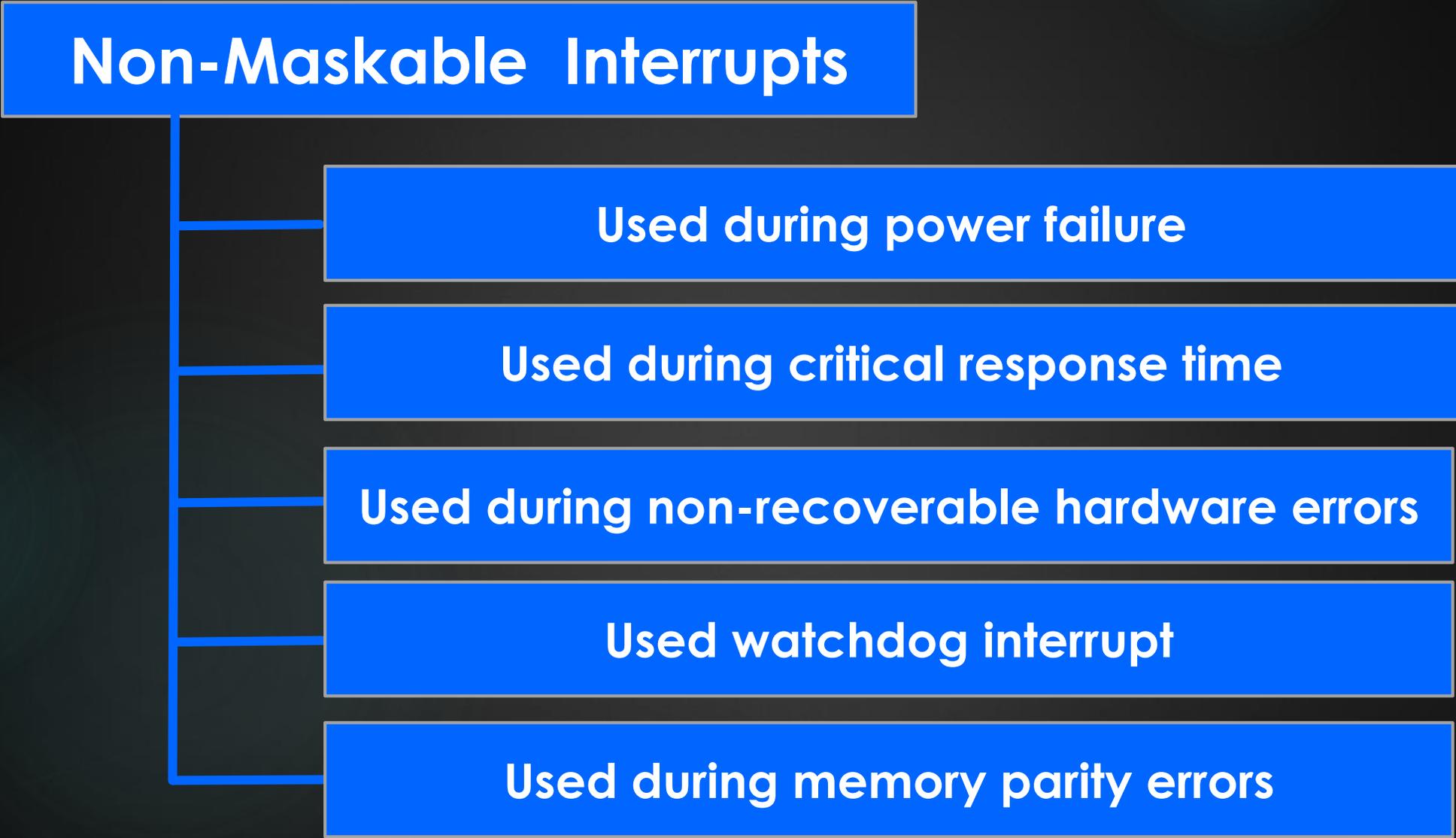
Maskable & Non-Maskable Interrupts



Maskable & Non-Maskable Interrupts



Non-Maskable Interrupts



Used during power failure

Used during critical response time

Used during non-recoverable hardware errors

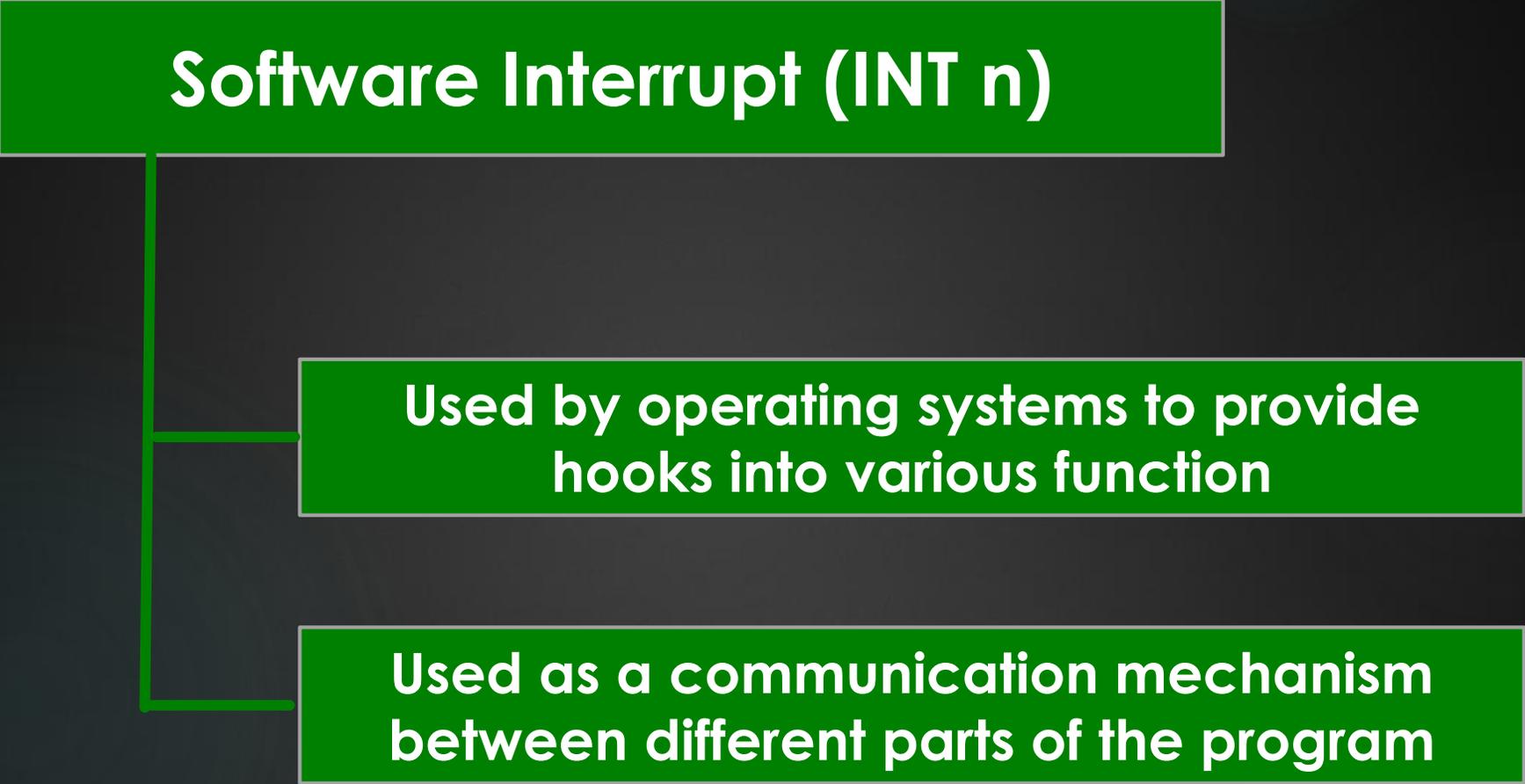
Used watchdog interrupt

Used during memory parity errors

Software Interrupts

The software interrupts are program instructions. These instructions are inserted at desired locations in a program. While running a program, if software interrupt instruction is encountered then the processor initiates an interrupt. The 8086 processor has 256 types of software interrupts. The software interrupt instruction is INT n, where n is the type number in the range 0 to 255.

Software Interrupt (INT n)



Used by operating systems to provide hooks into various function

Used as a communication mechanism between different parts of the program

8086 INTERRUPT TYPES

256 INTERRUPTS OF 8086 ARE DIVIDED IN TO 3 GROUPS

1. TYPE 0 TO TYPE 4 INTERRUPTS-

These Are Used For Fixed Operations And Hence Are Called Dedicated Interrupts

2. TYPE 5 TO TYPE 31 INTERRUPTS

Not Used By 8086, reserved For Higher Processors Like
80286
80386 Etc

3. TYPE 32 TO 255 INTERRUPTS

Available For User, called User Defined Interrupts These Can Be H/W Interrupts And Activated Through Intr Line Or Can Be S/W Interrupts.

➤ **Type – 0 Divide Error Interrupt**

Quotient Is Large Cant Be Fit In Al/Ax Or Divide By Zero

➤ **Type –1 Single Step Interrupt**

Used For Executing The Program In Single Step Mode By Setting Trap Flag

➤ **Type – 2 Non Maskable Interrupt**

This Interrupt Is Used For Execution Of NMI Pin.

➤ **Type – 3 Break Point Interrupt**

Used For Providing Break Points In The Program

➤ **Type – 4 Over Flow Interrupt**

Used To Handle Any Overflow Error.

Conclusion

The CPU executes program, as soon as a key is pressed, the Keyboard generates an interrupt. The CPU will response to the interrupt – read the data. After that returns to the original program. So by proper use of interrupt, the CPU can serve many devices at the “same time”

Reference

- Net
- “Advanced microprocessor & peripherals ”
by K.M Bhurchandi & A.K Ray

Thank You