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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ITT204 - MICROCONTROLLER AND EMBEDDED SYSTEMS

II YEAR/ IV SEMESTER

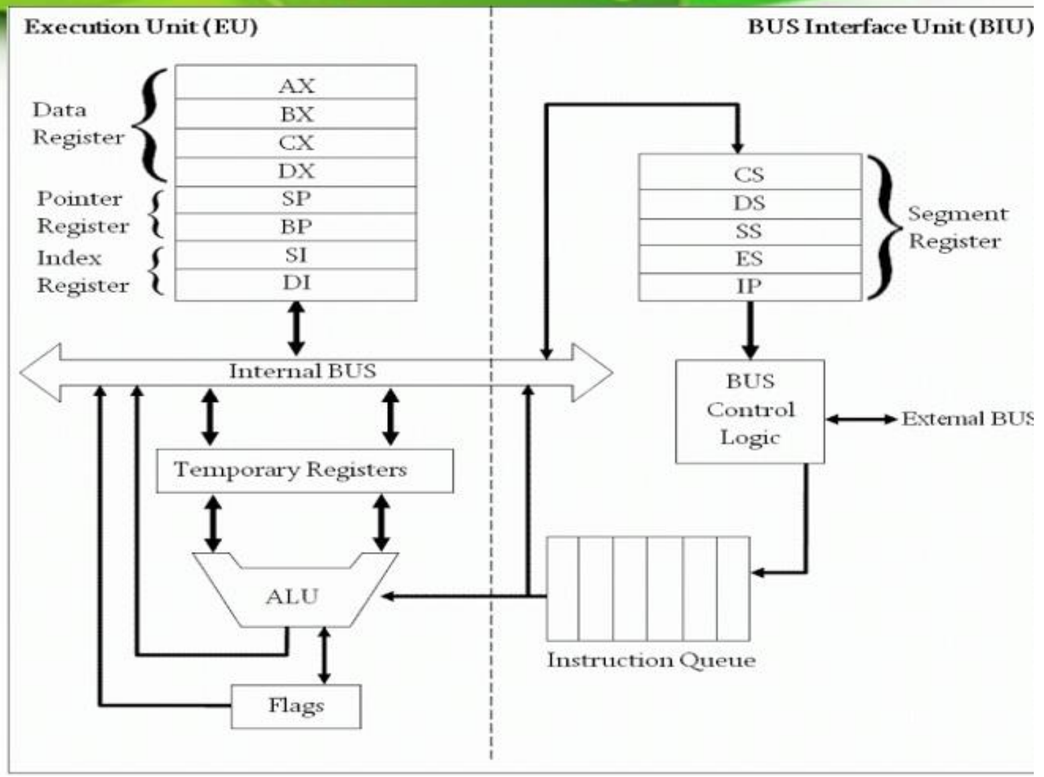
UNIT I ARCHITECTURE OF 8086 MICROPROCESSOR

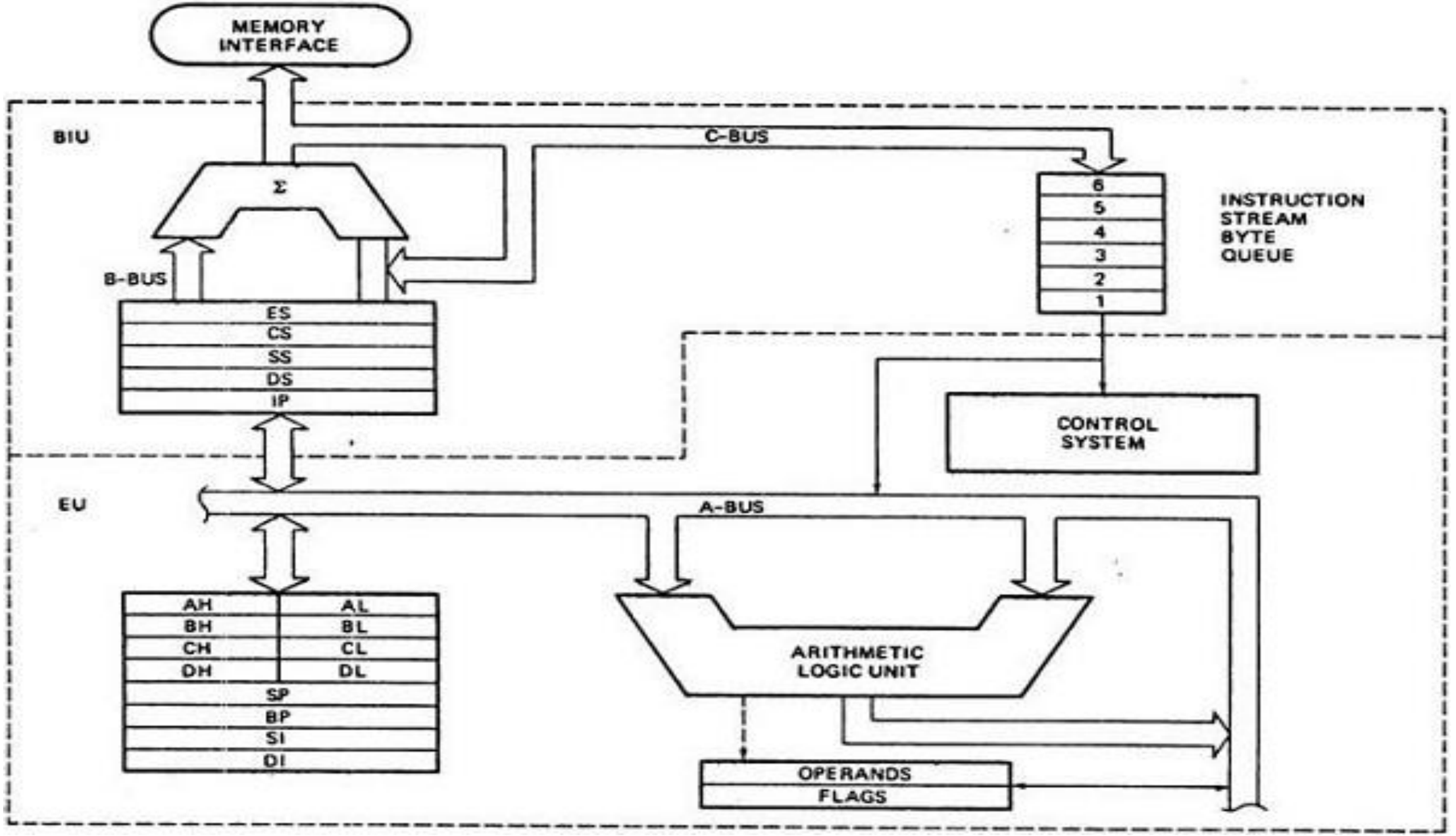
TOPIC – 8086 Internal Architecture

OUTLINE

INTERNAL ARCHITECTURE:

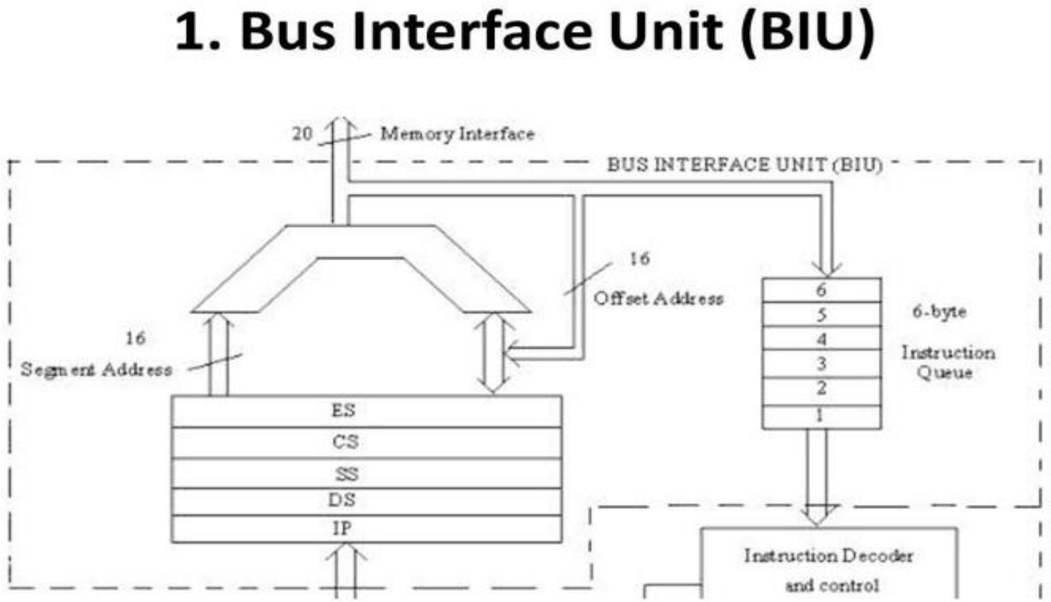
- 8086 has two blocks BIU and EU.
- BIU contains Instruction queue, Segment registers, Instruction pointer, Address adder.
- EU contains Control circuitry, Instruction decoder, ALU, Pointer and Index register, Flag register.




MEMORY INTERFACE
BIU
C-BUS
Σ
B-BUS
6
5
4
3
2
1
INSTRUCTION STREAM BYTE QUEUE
ES
CS
SS
DS
IP
CONTROL SYSTEM
EU
A-BUS
AH
AL
BH
BL
CH
CL
DH
DL
SP
BP
SI
DI
ARITHMETIC LOGIC UNIT
OPERANDS
FLAGS

Bus Interface Unit (BIU):

- The bus control logic of the BIU generates all the bus control signals such as read and write signals for memory and I/O.
- This unit handles all transfer of data and addresses on the buses for the EU(execution unit).



Bus Interface Unit (BIU):

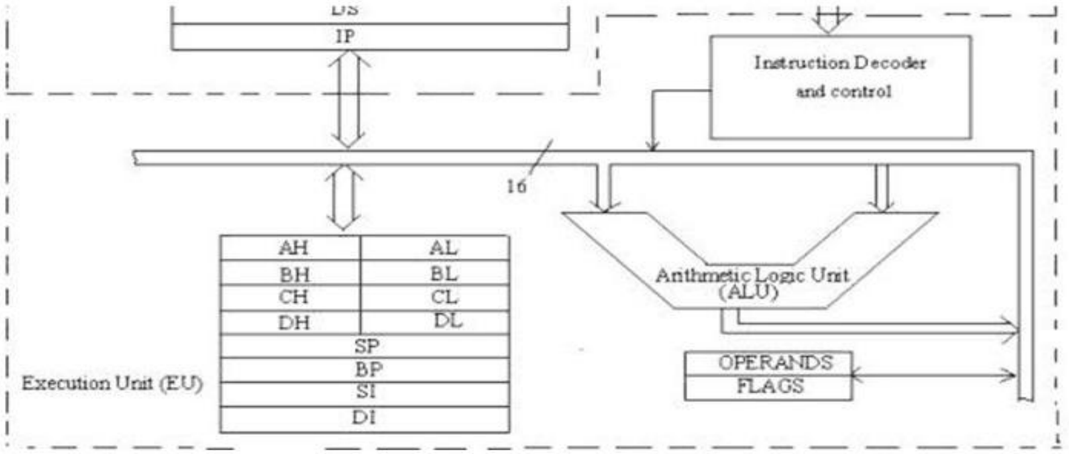
The function of BIU is to :

- Fetch the instruction or data from memory.
- Write the data to memory.
- Write the data to the port.
- Read data from the port.

Execution Unit (EU)

- Execution Unit also called a functional unit.
- An execution unit is a part of the central processing unit (CPU) that performs the operations and calculations as instructed by the computer program.

2. Execution Unit [EU]



Execution Unit (EU):

The functions of execution unit are :

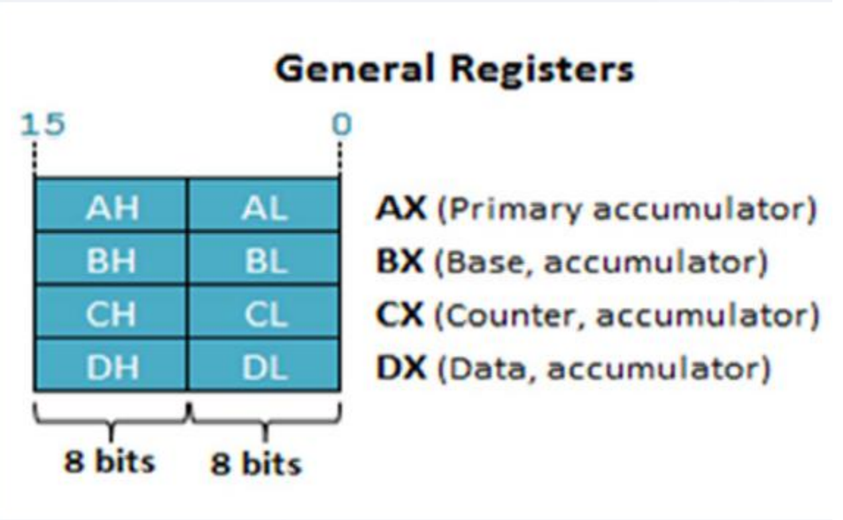
- To tell BIU where to fetch the instructions or data from.
- To decode the instructions.
- To execute the instructions.

Features of 8086 Microprocessor:

- It was the first 16-bit microprocessor.
- This microprocessor had major improvement over the execution speed of 8085.
- It is available as 40-pin Dual-Inline-Package (DIP).
- 8086 is designed to operate in two modes, Minimum and Maximum.
- It consists of 29,000 transistors.
- Address ranges from 00000H to FFFFFH.

General purpose registers:

- We have discussed general purpose registers as being discrete memory locations within the CPU used to hold temporary data and instructions.



❑ Type Of General Purpose Registers:

❖ AX - the accumulator register:

1. Arithmetic, logic and data transfer .
2. Multiplication & Division.
3. Input & Output.

❖ BX - the base address register:

1. BX register is an address register.
2. It usually contain a data pointer used for based, based indexed.

❑ Type Of General Purpose Registers:

❖ CX - the count register:

1. Iterative code segments using the LOOP instruction.
2. Repetitive operations on strings with the REP command.
3. Count (in CL) of bits to shift and rotate.

❖ DX - the data register:

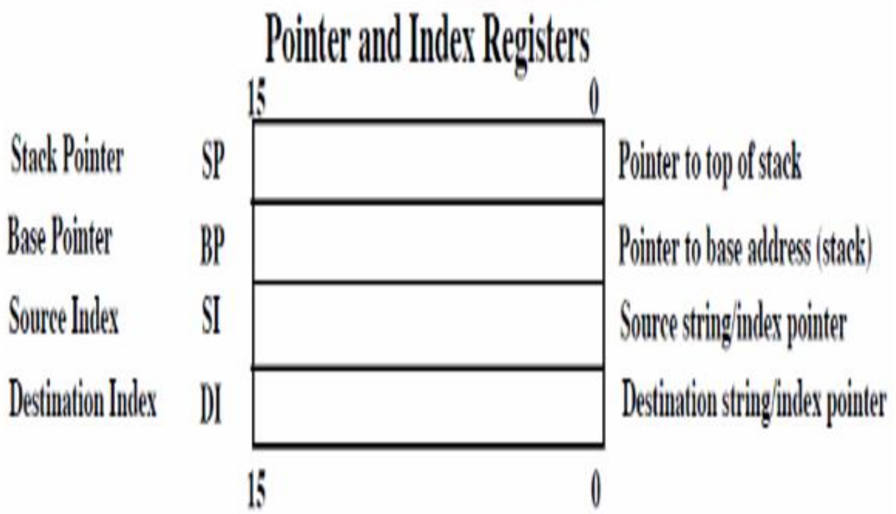
1. Data register can be used as a port number in I/O operations.
2. It is also used in multiplication and division.

❑ Pointers and index registers:

The pointers contain within the particular segments. The pointers IP, BP, SP usually contain offsets within the code, data and stack segments respectively.

❖ SI - source index register:

1. Can be used for pointer addressing of data.
2. Offset address relative to DS.



❑ Pointers and index registers:

❖ DI - destination index register:

1. Can be used for pointer addressing of data.
2. Offset address relative to ES.

❖ BP – base pointer:

1. Primarily used to access parameters passed via the stack.
2. Offset address relative to SS.

❖ SP - stack pointer:

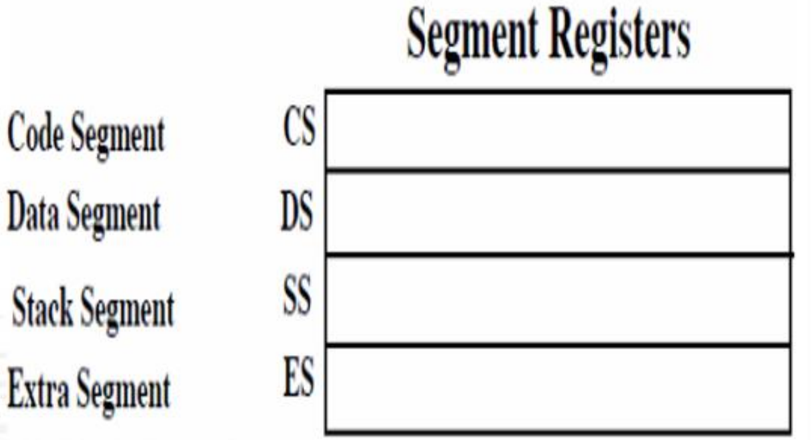
1. Always points to top item on the stack.
2. Offset address relative to SS.

Segment registers:

- In 8086/88 the processors have 4 segments registers:

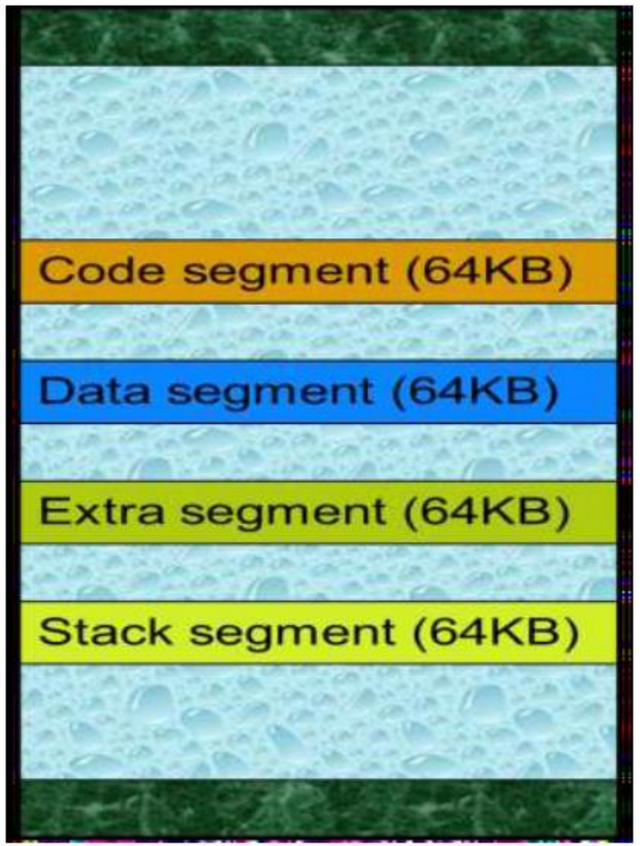
1. Code Segment register (CS) .
2. Data Segment register (DS).
3. Extra Segment register (ES) .
4. Stack Segment register (SS).

- All are 16 bit registers.



Segment Memory:

- The memory in an 8086 based system is Physical Memory organized as segmented memory.
- The CPU 8086 is able to address 1Mbyte of memory.
- The Complete physically available memory may be divided into a number of logical segments.



Function of segment register:

- CS - points at the segment containing the current program.
- DS - generally points at segment where variables are defined.
- ES - extra segment register, it's up to a coder to define its usage.
- SS - points at the segment containing the stack.

Advantages of Segmented Memory Scheme:

- Allows the memory capacity to be 1Mb.
- Allows the placing of code, data and stack portions of the same program in different parts.
- Permits a program to be put into different area.

❑ Special purpose register:

❖ IP - the instruction pointer:

1. Always points to next instruction to be executed.
2. Offset address relative to CS.

❖ IP register always works together with CS segment register and it points to currently executing instruction.

❑ FLAG REGISTERS:

The 8086 flag register contents indicate the results of computation in the ALU. It also contains some flag bits to control the CPU operations.

A 16 flag register is used in 8086. It is divided into two parts.

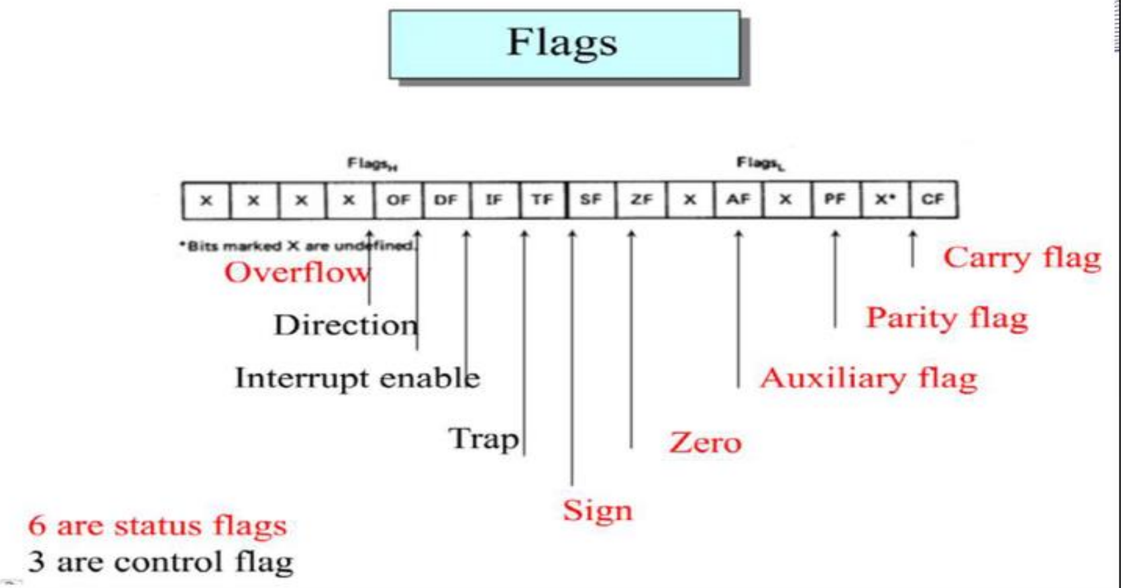
- ❖ Condition code or status flags- The condition code flag register is the lower byte of the 16-bit flag register.

- ❖ Machine control flags- The control flag register is the higher byte of the flag register. It contains three flags namely direction flag(D), interrupt flag (I) and trap flag (T).

❑ FLAG REGISTERS:

In EU the 8086 contains 16 bit Flag register. 9 of the 16 are active Flags and remaining 7 are undefined.

1. 6 Flags indicates some conditions – Status or Conditional Flags.
2. 3 Flags – Control Flags.



THANK YOU