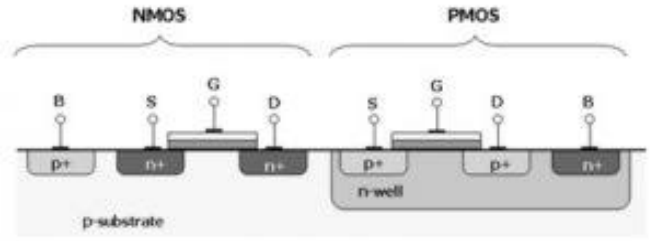
CMOS (Complementary Metal Oxide Semiconductor)

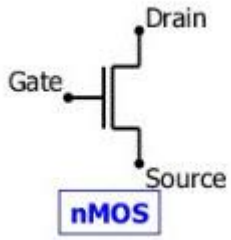
The main advantage of CMOS over NMOS and BIPOLAR technology is the much smaller power dissipation. Unlike NMOS or BIPOLAR circuits, a Complementary MOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. This allows integrating more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance. Complementary Metal Oxide Semiconductor transistor consists of P-channel MOS (PMOS) and N-channel MOS (NMOS). Please refer to the link to know more about the fabrication process of CMOS transistor.



CMOS (Complementary Metal Oxide Semiconductor)

NMOS

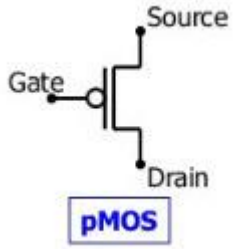
NMOS is built on a p-type substrate with n-type source and drain diffused on it. In NMOS, the majority of carriers are electrons. When a high voltage is applied to the gate, the NMOS will conduct. Similarly, when a low voltage is applied to the gate, NMOS will not conduct. NMOS is considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel twice as fast as the holes.



NMOS Transistor

PMOS

P- channel MOSFET consists of P-type Source and Drain diffused on an N-type substrate. The majority of carriers are holes. When a high voltage is applied to the gate, the PMOS will not conduct. When a low voltage is applied to the gate, the PMOS will conduct. The PMOS devices are more immune to noise than NMOS devices.

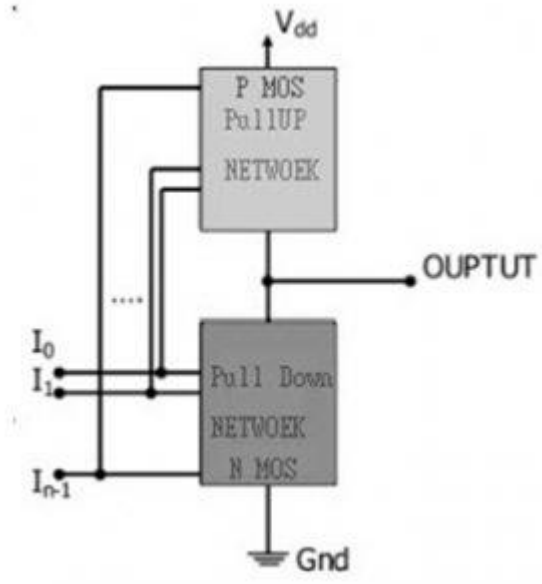


PMOS Transistor

CMOS Working Principle

In CMOS technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor.

In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (Vss or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named Vdd).



CMOS using Pull Up & Pull Down

Thus, if both a p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern as shown in the figure below.

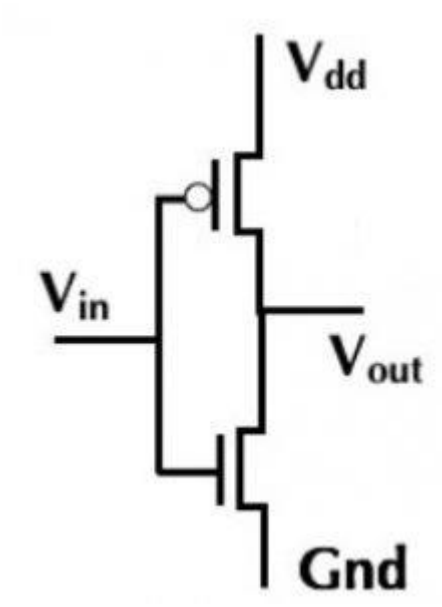
CMOS offers relatively high speed, low power dissipation, high noise margins in both states, and will operate over a wide range of source and input voltages (provided the source voltage is fixed). Furthermore, for a better understanding of the Complementary Metal Oxide Semiconductor working principle, we need to discuss in brief CMOS logic gates as explained below.

Which Devices use CMOS?

Technology like CMOS is used in different chips like microcontrollers, microprocessors, SRAM (static RAM) & other digital logic circuits. This technology is used in a wide range of analog circuits which includes data converters, image sensors & highly incorporated transceivers for several kinds of communication.

CMOS Inverter

The inverter circuit as shown in the figure below. It consists of PMOS and NMOS FET. The input A serves as the gate voltage for both transistors.
The NMOS transistor has input from Vss (ground) and the PMOS transistor has input from Vdd. The terminal Y is output. When a high voltage (~ Vdd) is given at input terminal (A) of the inverter, the PMOS becomes an open circuit, and NMOS switched OFF so the output will be pulled down to Vss.



CMOS Inverter

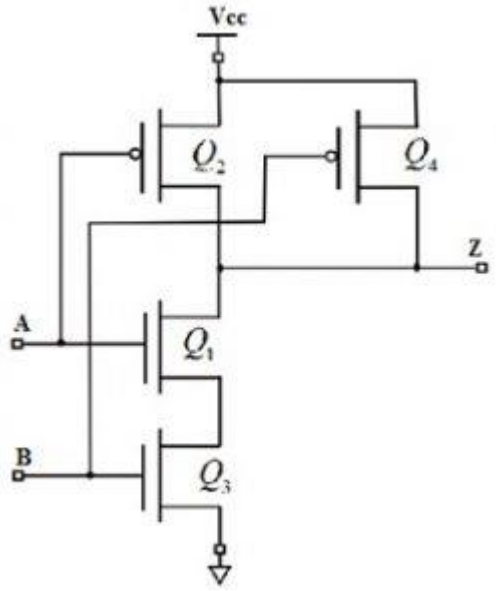
When a low-level voltage (<Vdd, ~0v) applied to the inverter, the NMOS switched OFF and PMOS switched ON. So the output becomes Vdd or the circuit is pulled up to Vdd.

INPUT	LOGIC INPUT	OUTPUT	LOGIC OUTPUT
0 v	0	Vdd	1
Vdd	1	0 v	0

CMOS NAND Gate

The below figure shows a 2-input Complementary MOS NAND gate. It consists of two series NMOS transistors between Y and Ground and two parallel PMOS transistors between Y and VDD.

If either input A or B is logic 0, at least one of the NMOS transistors will be OFF, breaking the path from Y to Ground. But at least one of the pMOS transistors will be ON, creating a path from Y to VDD.



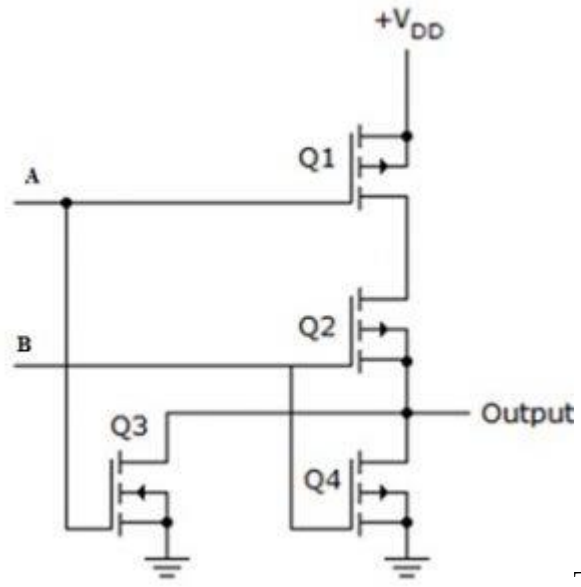
Two Input NAND Gate

Hence, the output Y will be high. If both inputs are high, both of the nMOS transistors will be ON and both of the pMOS transistors will be OFF. Hence, the output will be logic low. The truth table of the NAND logic gate given in the below table.

A	B	Pull-Down Network	Pull-up Network	OUTPUT Y
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

CMOS NOR Gate

A 2-input NOR gate is shown in the figure below. The NMOS transistors are in parallel to pull the output low when either input is high. The PMOS transistors are in series to pull the output high when both inputs are low, as given in the below table. The output is never left floating.



Two Input NOR Gate

The truth table of the NOR logic gate given in the below table.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

CMOS Characteristics

The most important characteristics of CMOS are low static power utilization, huge noise immunity. When the single transistor from the pair of MOSFET transistor is switched OFF then the series combination uses significant power throughout switching among the two stated like ON & OFF.

Advantages

- It uses a single power supply like + VDD
- These gates are very simple
- Input impedance is high
- CMOS logic uses less power whenever it is held in a set state
- Power dissipation is negligible
- Fan out is high
- TTL compatibility
- Stability of temperature
- Noise immunity is good
- Compact
- Designing is very well

- Robust mechanically
- Logic swing is large (VDD)

Disadvantages

The disadvantages of CMOS include the following.

- The cost will be increased once the processing steps increases, however, it can be resolved.
- The packing density of CMOS is low as compared with NMOS.
- MOS chips should be secured from getting static charges by placing the leads shorted otherwise; the static charges obtained within leads will damage the chip. This problem can be solved by including protective circuits otherwise devices.
- Another drawback of the CMOS inverter is that it utilizes two transistors as opposed to one NMOS to build an inverter, which means that the CMOS uses more space over the chip as compared with the NMOS. These drawbacks are small due to the progress within the CMOS technology.

CMOS Applications

Complementary MOS processes were widely implemented and have fundamentally replaced NMOS and bipolar processes for nearly all digital logic applications. CMOS technology has been used for the following digital IC designs.

- Computer memories, CPUs
- Microprocessor designs
- Flash memory chip designing
- Used to design application-specific integrated circuits (ASICs)