What is Emitter Coupled Logic?

Emitter-coupled logic is the best BJT-based logic family used in the conventional logic-system design. Sometimes, it is also called current mode logic which is a very high-speed digital technology. Generally, ECL is considered as the fastest logic IC where it achieves its high-speed operation by using a very small voltage swing & also avoiding the transistors from entering the saturation region.

An implementation of ECL utilizes a positive supply voltage which is known as PECL or positive-referenced ECL. In early ECL gates, a negative voltage supply is used due to the noise immunity. After that, positive-referenced ECL became very famous due to its more compatible logic levels as compared to TTL logic families.

Emitter-coupled logic dissipates a huge amount of static power, however, its overall consumption of current is low as compared to CMOS at high frequencies. So, ECL is mainly beneficial in clock-distribution circuits & high-frequency-based applications.

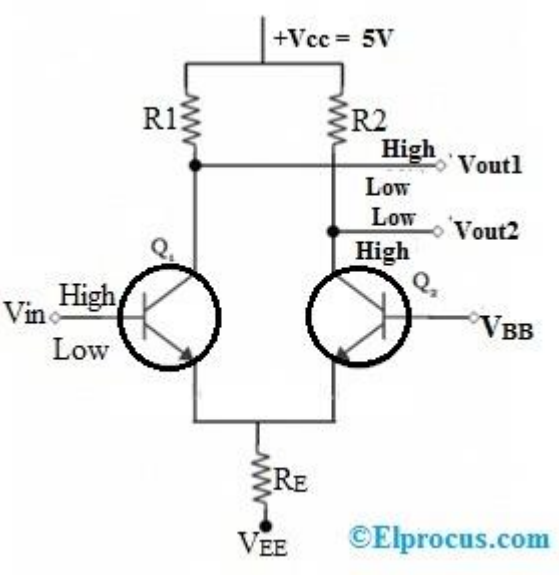
Emitter Coupled Logic Features

The features of ECL will make them used in many high-performance-based applications.

- ECL provides two outputs which are complements of each other always because, the operation of the circuit is based on a differential amplifier.
- This logic family is mainly suitable for monolithic fabrication methods because logic levels are a function of resistor ratios.
- The devices of the ECL family generate the right & complementary output of the proposed function without using any outside inverters. Consequently, it decreases the package count, and requirements of power & also decreases problems occurring from time delays.
- ECL devices in differential amplifier design offer broad performance flexibility, so ECL circuits allow being used both as digital and linear circuits.
- The design of the ECL gate has normally high & low input impedance, which is extremely conducive to attaining large fan-out as well as drive capability.
- ECL devices generate a constant current drain on the power supply to simplify the design of the power supply.
- The devices of ECL including open emitter outputs simply allow them to include transmission line drive capacity.

Emitter Coupled Logic Circuit

The emitter-coupled logic circuit for the inverter is shown below which is designed with resistors and transistors. In this circuit, the emitter terminals of two transistors are simply connected to current limiting resistance RE which is used to avoid the transistor from entering into saturation. Here the transistor's output is taken from the collector terminal instead of the emitter terminal. This circuit provides two outputs Vout (inverting output) and Vout2 (non-inverting output) and the input terminal like Vin where high or low input is given. +Vcc = 5V.



Emitter Coupled Logic Circuit

How Does Emitter Coupled Logic Work?

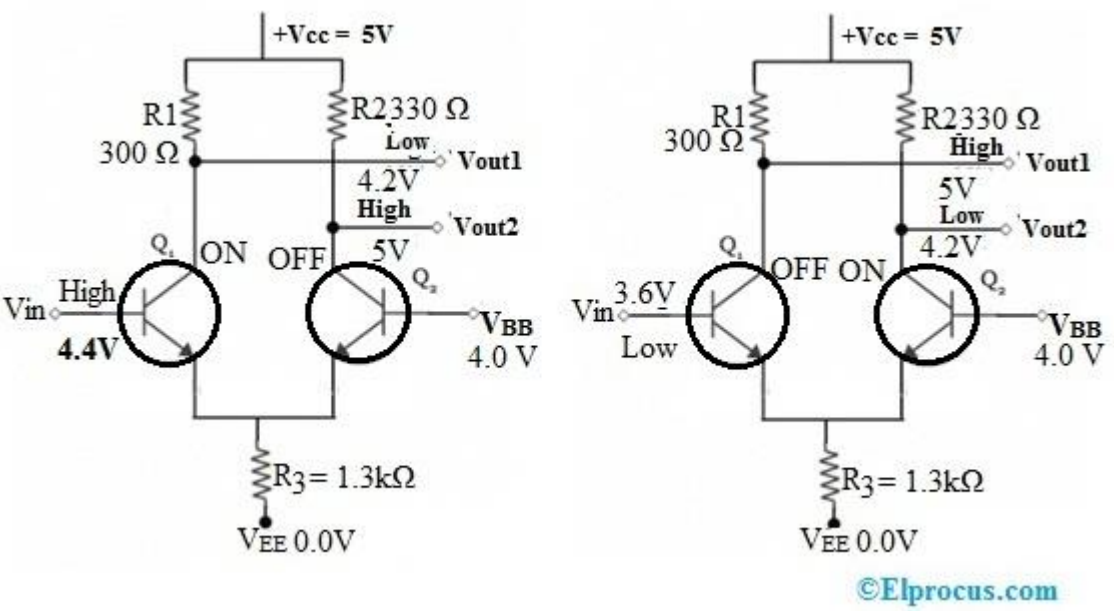
The operation of emitter-coupled logic is, that whenever the HIGH input is given to the ECL circuit, then it will make the 'Q1' transistor ON and the Q2 transistor OFF but the Q1 transistor is not saturated. So this will pull the VOUT2 output to HIGH and the value of VOUT1 output will be LOW because of the drop within R1.

Similarly, when the VIN value given to ECL is LOW, then it will make the Q1 transistor OFF & Q2 transistor ON. So, the Q2 transistor will not move into saturation. So it will make the VOUT1 output to be pulled HIGH value and the VOUT2 output value will be low because of the drop within R2 resistance.

Let see how the transistor Q1 and Q2 turns on and off when a voltage is applied.

The two transistors like Q1 & Q2 in this circuit are connected as a differential amplifier by a common emitter resistor.

The voltage supplies for this example circuit are VCC = 5.0, VBB = 4.0 & VEE = 0 V. The input HIGH & LOW-level values are simply defined to be 4.4 V & 3.6V. Actually, this circuit generates LOW output & HIGH levels that are 0.6 Volts higher; however, this is corrected within real ECL circuits.



Emitter Coupled Logic Example

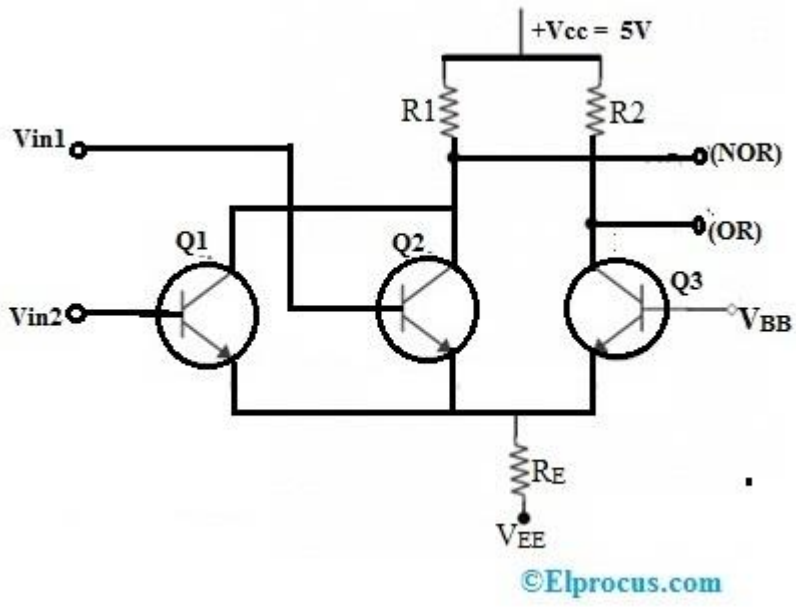
Once Vin is HIGH, then the Q1 transistor is turned on, however not saturated & the Q2 transistor is turned off. So, output voltage like VOUT2 is pulled to 5 V through the R2 resistor & it can be shown that the voltage drop across the R1 resistor is about 0.8 V so that VOUT1 = 4.2 V (LOW). In addition VE = VOUT1 – VQ1 => 4.2V – 0.4V = 3.8V as transistor Q1 is turned ON completely.

Once Vin is LOW, the Q2 transistor will be turned on, but not saturated & the Q1 transistor is turned OFF. Therefore, VOUT1 is pulled to 5.0 V using an R1 resistor & it can be shown that VOUT2 is 4.2 V. Also VE => VOUT2 – VQ2 => 4.2V – 0.8V => 3.4V as transistor Q2 is turned ON.

In ECL, the two transistors are never in saturation as t**he input / output voltage swings are fairly small like 0.8v** and the input impedance is high and output resistance is low. This helps ECL to operate faster with a less propagation delay time.

Two Input Emitter Coupled Logic OR/NOR Gate Circuit

The two input emitter coupled logic OR/NOR gate circuit is shown below. This circuit is designed by modifying the above inverter circuit. The modification is by adding an extra transistor at the input side.
The working of this circuit is very simple. When the inputs applied at both the Q1 & Q2 transistors are low then will make the output1 (Vout1) to a HIGH value. So, this Vout1corresponds to the output of the NOR gate.



Two Input ECL OR NOR Gate

Simultaneously, if the Q3 transistor is turned ON, then it will make the second output (Vout2) to be HIGH. So, this Vou2 output corresponds to the OR gate output.

In the same way, if both the Q1 &Q2 transistors inputs are HIGH, then it will turn on the Q1 & Q2 transistors and provides the low output at the VOUT1 terminal.

If the Q3 transistor is turned OFF throughout this operation then it will provide high output at the VOUT2 terminal. So, the truth table for OR/NOR gate is given below.

Inputs	Inputs	OR	NOR
A	B	Y	Y
0	0	0	1
0	1	1	0
1	0	1	0

1	1	1	0

Emitter-Coupled Logic Characteristics

The characteristics of ECL include the following.

- As compared to TTL, ECL has a faster propagation time ranging from 0.5 to 2 ns. But, emitter coupled logic power dissipation is higher as compared to TTL like 30 mW.
- The I/O voltages of ECL have a small swing like 0.8.
- The input impedance of ECL is high & the output resistance is low; consequently, the transistor changes its states very fast.
- ECLs fan-out capacity is high and gate delays are low.
- The o/p logic of ECL changes from a LOW to a HIGH state but the levels of voltage for these states will vary between TTL & EC.
- The noise immunity of ECL is 0.4V.

Advantages and Disadvantages

The **advantages of emitter-coupled logic** are discussed below.

- The fanout of ECL is 25 which is better as compared to TTL & it is low as compared to CMOS.
- The average propagation delay time of ECL is 1 to 4 ns which is better as compared to both CMOS &
- TTL. Thus it is called as fastest logic family.
- When the BJTs in emitter coupled logic gates work in the active region, then they have the maximum speed as compared to all logic families.
- ECL gates generate complementary outputs.
- Current switching spikes are not there in the power supply leads.
- Outputs can be coupled jointly to provide the wired-OR function.
- The parameters of ECL do not change much through temperature.
- The no. of functions accessible from an only chip is high.

The **disadvantages of emitter-coupled logic** are discussed below.

- It has an extremely less noise margin i.e, ±200 mV.
- Power dissipation is high as compared to other logic gates.
- To interface with other logic families, level shifters are necessary.
- Fanout limits capacitive loading.
- As compared to TTL, ECL gates are expensive.
- As compared to CMOS & TTL, ECL noise immunity is worst.

Applications

The applications of emitter-coupled logic include the following.

- Emitter-coupled logic is used as a logic & interface technology within extremely high-speed communications devices like fiber-optic transceiver interfaces, Ethernet & ATM (Asynchronous Transfer Mode) networks.
- ECL is a logic family based on BJT where its high-speed operation can be achieved by using a relatively small voltage swing & avoiding the transistors from moving into the saturation region.
- ECL is used in making the ASLT circuits within the IBM 360/91.
- ECL avoids the utilization of stacked transistors by using a single-ended bias i/p & positive feedback between primary & secondary transistors to attain an inverter function.
- ECL is used in extremely high-speed electronics.