# What is Ring Counter?

Definition: A ring counter is also known as SISO (<u>serial in serial out</u>) shift register counter, where the output of the flip flop is connected to the input of the flip flop which acts as a ring counter. The designing of the ring counter can be done by using four <u>D-Flip Flops</u> with a common clock signal and overriding input can be connected to pre-set and clear.
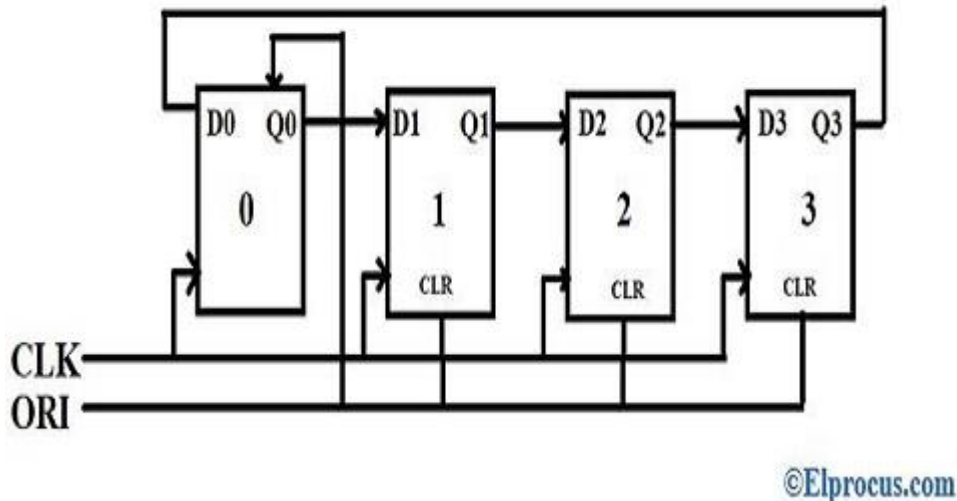
block-diagram-of-ring-counter

From the above diagram,

1). The number of states used is 4 (Where no of states = no of flip flops used).

2). Pre-set or Clear: The main function of this is if the input clock signal changes then the output value is also changed.

The connections are made as follows

- One input is connected to the first flip-flop ff0-Q0,
- Another input is connected to CLR of the other three flip flops like ff1, ff2, ff3.

Working Theory

For example, let us take a condition where pre-set = '0000' then the outputs obtained at each flip flop is as follows. For FF0, the output at Q0 is '1',

whereas in other flipflops like ff, ff2, ff3 (which are connected to clear where CLR = 0) the outputs obtained at Q1 = Q2 = Q3 ='0'. This can be understood by following the truth table and its output waveforms obtained when executed using Verilog HDL code in

Truth Table

ORI	CLK	Q0	Q1	Q2	Q3
Low Pulse	X	1	0	0	0
1	0	0	1	0	0
1	0	0	0	1	0
1	0	0	0	0	1
1	0	1	0	0	0

Where

Inputs = ORI and CLK

X = Clock can be either a positive edge or a negative edge

Outputs = Q0, Q1, Q2, Q3.

From the table, we can observe that '1' is shifted diagonally from Q0 to Q3 and again will shifts back to 'Q0'. So this shows that it works like a ring counter.
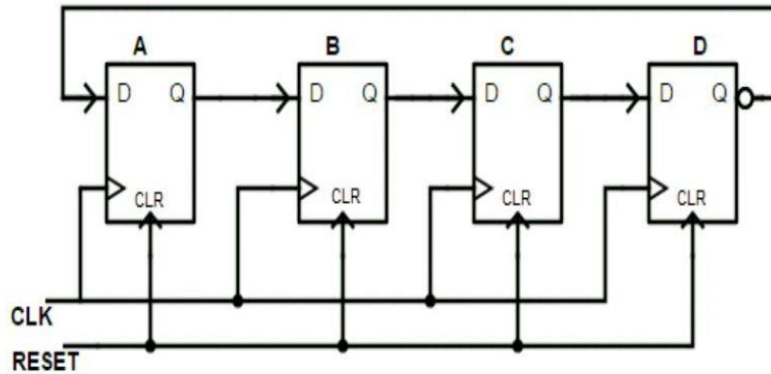
What is Johnson Counter?

Definition: It is also known as a modified ring counter. It is designed with a group of flip-flops, where the inverted output from the last flip-flop is connected to the input of the first flip-flop. Generally, it is implemented by using D flip-flops or JK flip-flops. It is also known as an inverse feedback counter or twisted ring counter. This follows the sequence of bit patterns. When compared to the ring counter, it uses only half of the number of flip-flops. So, the MOD will be 2n, if there are n flip-flops.

Circuit Diagram

The **johnson counter circuit diagram** is the cascaded arrangement of 'n' flip-flops. In such design, the output of the proceeding flip-flop is fed back

as input to the next flip-flop. For example, the inverted output of the last flip-flop 'Q̄n' is fed back to the first flip-flop in the sequence bit pattern. The counter registers cycles in a closed-loop i.e circulates within the circuit.

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Consider the 4-bit Johnson counter, it contains 4 D flip-flops, which is called 4-bit Johnson counter. It has preset and clear pins to initialize or start and reset the counted.

Reset pin acts as an on/off switch. So, the flip-flops can be enabled by clicking the Reset switch.

CLK pin is used to observe the changes in the output of the flip-flops.

Standard 2,3 and 4 stages johnson counters are used to divide the frequency of clock signals with the help of varying feedback connections. For example, a 3-stage johnson counter can be used as a 3-phase and 120 degrees phase shift square wave generator. 5-stage Johnson counter is used as a synchronous decade counter (CD4017) or divider circuit. 2-stage acts as a quadrature oscillator or generator that produces individual output signals of 90 degrees each concerning the input signal.

Truth Table

Consider the truth table of the 3-bit Johnson counter. The output of the proceeding flip-flop is connected as the input of the next flip-flop. The clock signal(CLK) is used to know the changes in the output. It contains 3 flip-flops, Q_0, Q_1, Q_2 are the outputs of the flip-flops. The counter counts the state of cycles in a continuous closed loop.

State	Q0	Q1	Q2
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1

The input D is just before the rising edge of the clock (CLK), denoted as Q0.

When the CLK rising edge occurs, the output Q1 is the value of Q0.

When there is no clock pulse (0), the output of the counter is 000.

When CLK=1, the output of the counter is 100.When CLK=2, the output of the counter is 110.When CLK=3, the output of the counter is 111.When CLK=4, the output of the counter is 011.When CLK=5, the output of the counter is 001.

The MOD of the 3-bit johnson counter is 6. Hence there are 6 uniques numbers of states. The complete process is in the sequence bit pattern.