SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

19ECB231-DIGITAL ELECTRONICS

II YEAR/ III SEMESTER

UNIT 5 – SEQUENTIAL CIRCUITS

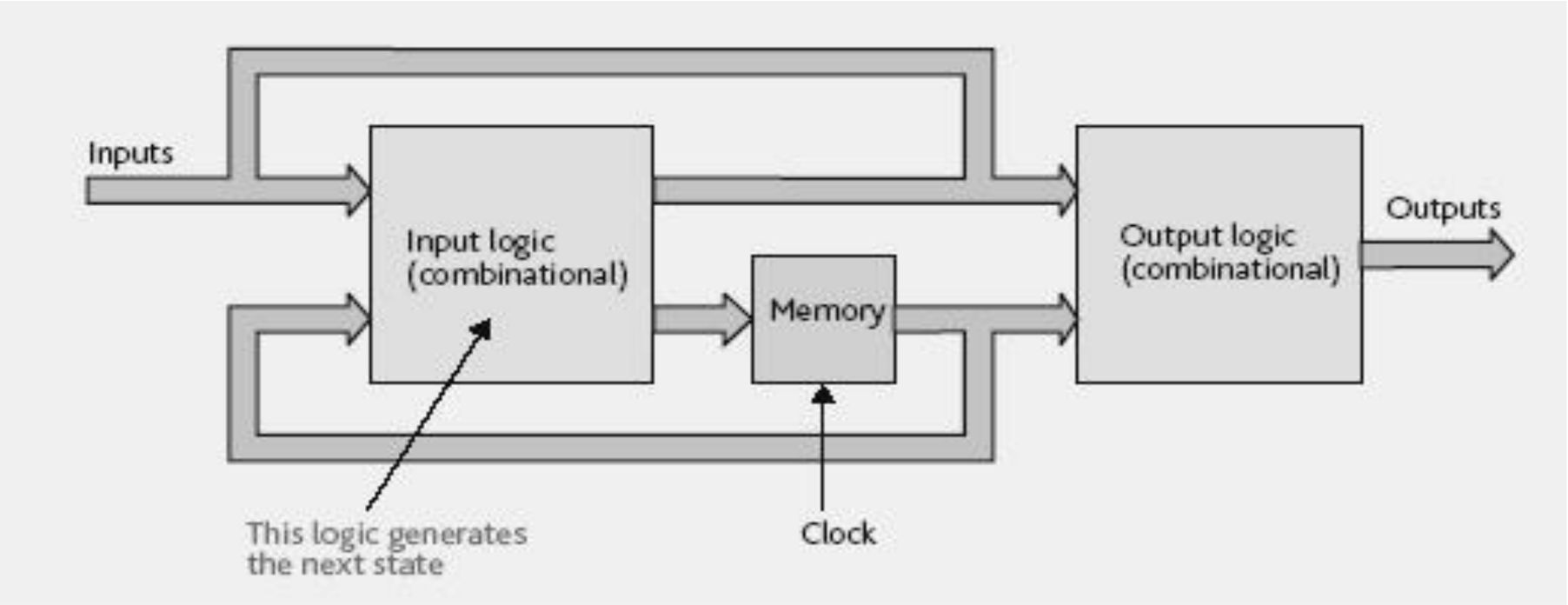
TOPIC 4 – Analysis and design of clocked sequential circuits – Moore/Mealy models

Classification of SLC

- The sequential circuits can be classified into two categories depending on the timing of their signals
  - Synchronous sequential logic circuit
  - Asynchronous sequential logic circuit
- In case of synchronous sequential circuits, it is assumed that the behavior of the system synchronized by a clock.
- The system behavior is determined by the values of present state and external input signals at discrete instants of time.
- In case of asynchronous sequential logic circuits the order in which input signals change affected network behavior.
- Further more, these changes are allowed to occur at any instant of time.

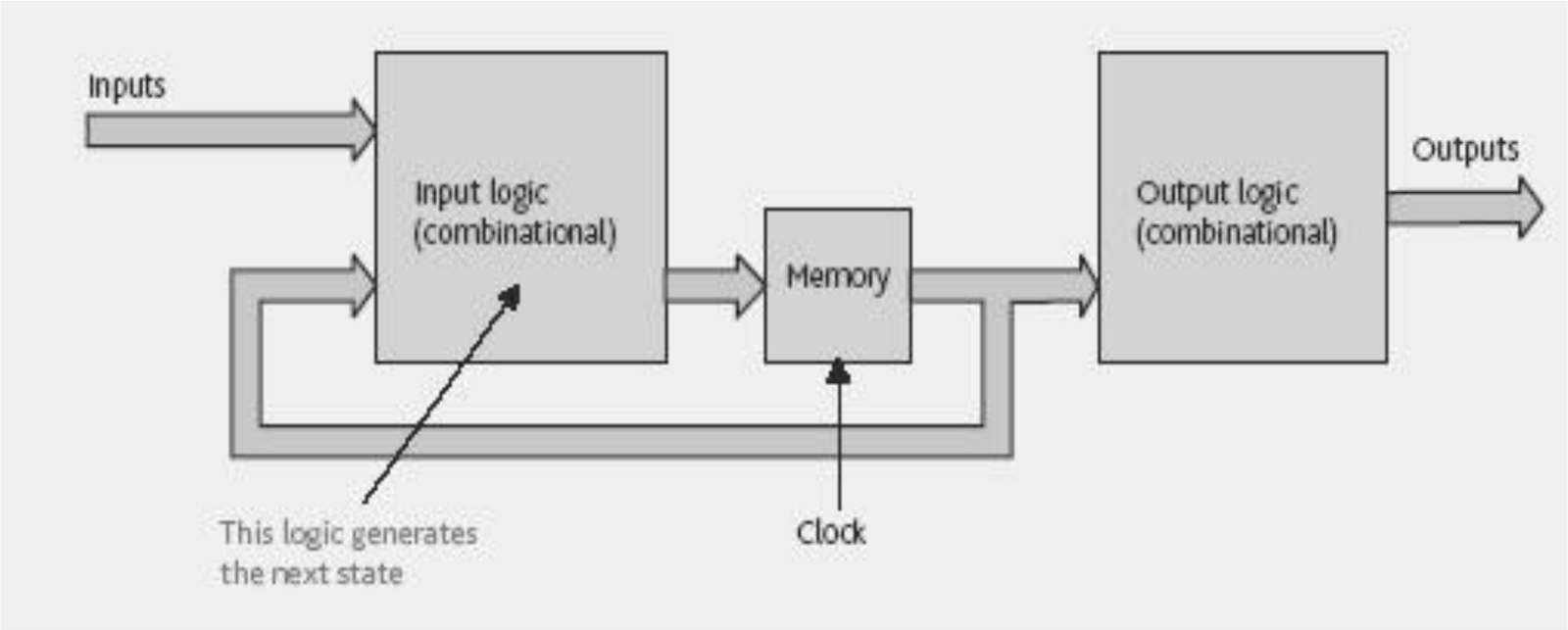
Mealy Model

- The figure shows the clocked synchronous sequential Mealy machine.
- The output of mealy machine is the function of present inputs and present state (Flip flop outputs).



Moore Machine

- The figure shows the block diagram of a Moore machine.
- The output of Moore machine depends only on the present state.
- So the output of Moore machine is a function of its present state



Difference between Moore and Mealy Machine

SNo.	*Moore machine*	*Mealy machine*
1.	The output of this machine is the function of the present state only	Its output is function of input as well as present state present
2.	Input changes do not affect the output	Input changes may affect the output
3.	It requires more number of states for implementing same function	It requires less number of states for implementing same function
4	Speed is high	Speed is low
5	Design process is very complicate	Less complex than Moore design

Synchronous Sequential Circuit Models

Structural „

•Logic diagram „

• Excitation Equations „

• Output equations

Behavioral „

•Transition and output equations „

•Transition table „

• State table „

• State diagram (graph)

•$SC Analysis: Derive one of the behavioral models from an instance of a structural model

$SC Synthesis: Derive a structural model from one of the behavioral models

ANALYSIS OF SYNCHRONOUS SEQUENTIAL CIRCUITS

•The behavior of sequential circuit can be determined from the inputs, the output and state of its flip flops.

•The outputs and next state are both a function of its inputs and the present state.

•The analysis of a sequential circuit consists of obtaining a table or diagram for the time sequence of inputs, outputs and internal states.

Analysis Procedure

- Identify type of circuit either Mealy or Moore circuit
- Derive excitation equation (Boolean expression)
- Derive next state and output equations
- Generate state table
- Generate state diagram

Analysis Procedure

DESIGN PROCEDURE FOR CLOCKED SEQUENTIAL CIRCUIT

The following steps are followed to design the clocked sequential logic circuit.

•Obtain the state table from the given circuit information such as a state diagram, a timing diagram or description.

•The number of states may be reduced by state reduction technique.

•Assign binary values to each state in the state table.

•Determine the number of flip flops required and assign a letter symbol to each flip flop.

•Choose the flip flop type to be used according to the application.

•Derive the excitation table from the reduced state table.

•Derive the expression for flip flop inputs and outputs using k-map simplification (The present state and inputs are considered for k-map simplification) and draw logic circuit

THANK YOU