# SNS COLLEGE OF TECHNOLOGY

**Coimbatore-35**
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# DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## 19ECB231 –DIGITAL ELECTRONICS

II YEAR/ III SEMESTER

## UNIT 5 – SEQUENTIAL CIRCUITS

TOPIC 5 – Analysis and design of clocked sequential circuits – Moore/Mealy models example

# Analysis Procedure

- Identify type of circuit either Mealy or Moore circuit
- Derive excitation equation (Boolean expression)
- Derive next state and output equations
- Generate state table
- Generate state diagram

# Analysis Procedure

**DESIGN PROCEDURE FOR CLOCKED SEQUENTIAL CIRCUIT**

The following steps are followed to design the clocked sequential logic circuit.

- Obtain the state table from the given circuit information such as a state diagram, a timing diagram or description.
- The number of states may be reduced by state reduction technique.
- Assign binary values to each state in the state table.
- Determine the number of flip flops required and assign a letter symbol to each flip flop.
- Choose the flip flop type to be used according to the application.
- Derive the excitation table from the reduced state table.
- Derive the expression for flip flop inputs and outputs using k-map simplification (The present state and inputs are considered for k-map simplification) and draw logic circuit

# Analysis of Sequential Logic

1. **Analysis is the process that starts with an implementation and generates the function or behavior of the sequential** circuit.

   i.e. given a logic schematic, to generate one or more functional descriptions, using state diagrams, state and output tables, and input and output Boolean equations.

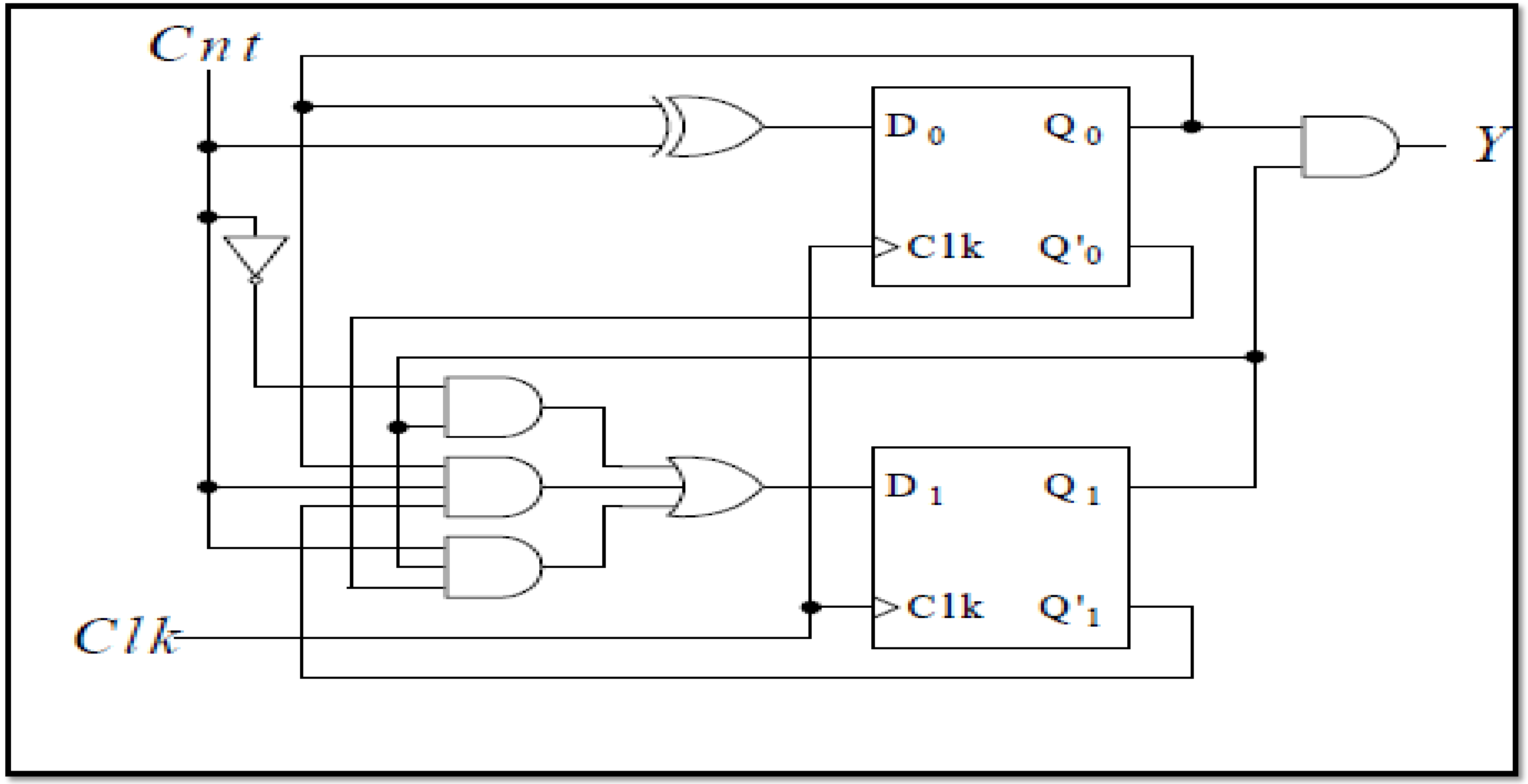
**2.Synthesis, the reverse of analysis, starts with a behavioral description and generates an implementation**

# Moore Machine

**<u>State-based or Moore-type sequential circuit.</u>**

**The output values depend solely on its present state.**

Derive the next state, the output tables, and the state diagram for the (modulo-4 counter) sequential circuit represented by the following schematic.



# Moore Machine

**Solution:**

**Step 1 (Moore):** Derive **excitation equations.**

i.e., boolean expressions for the inputs of each flip-flop in the schematic, in terms of the external input Cnt and the ff outputs Q1 and Q0.

Since there are two ffs in our example, we derive two expressions for D1 and D0:

$$D_0 = Cnt \oplus Q_0 = Cnt'Q_0 + CntQ_0'$$
$$D_1 = Cnt'Q_1 + CntQ_1'Q_0 + CntQ_1Q_0'$$

# Moore Machine

**Solution:**

Step 2:

Derive the **next-state equations by substituting the excitation equations into the flip-flop characteristic** equations.

The **characteristic equations formally describe the functional behavior of a latch or flip-flop.**

**They specify the** flip-flop's next state as a function of its current state and inputs.

For the D flip-flop, the characteristic equation is

***Qnext = D***

Thus, the next-state equations are:

$$Q_{0next} = D_0 = Cnt \oplus Q_0 = Cnt'Q_0 + CntQ_0'$$

$$Q_{1next} = D_1 = Cnt'Q_1 + CntQ_1'Q_0 + CntQ_1Q_0'$$

Step 2b (Moore):

Derive the **output equation.**

$$Y = Q_1Q_0$$

# Moore Machine

**Solution:**

Step 3a:

Derive the next-state table from the next-state equations.

Each row corresponds to a state of the sequential circuit which is defined by the binary values stored in its ffs.

Each column represents one set of input values.

Each entry defines the value of the sequential circuit in the next clock cycle after the rising edge of the Clk.

| Present State | Next State | | Outputs |
|---|---|---|---|
| $Q_1Q_0$ | $Q_{1\ next}\ Q_{0\ next}$ | | $Y$ |
| | $Cnt = 0$ | $Cnt = 1$ | |
| 00 | 00 | 01 | 0 |
| 01 | 01 | 10 | 0 |
| 10 | 10 | 11 | 0 |
| 11 | 11 | 00 | 1 |

# Moore Machine

**<u>Solution:</u>**

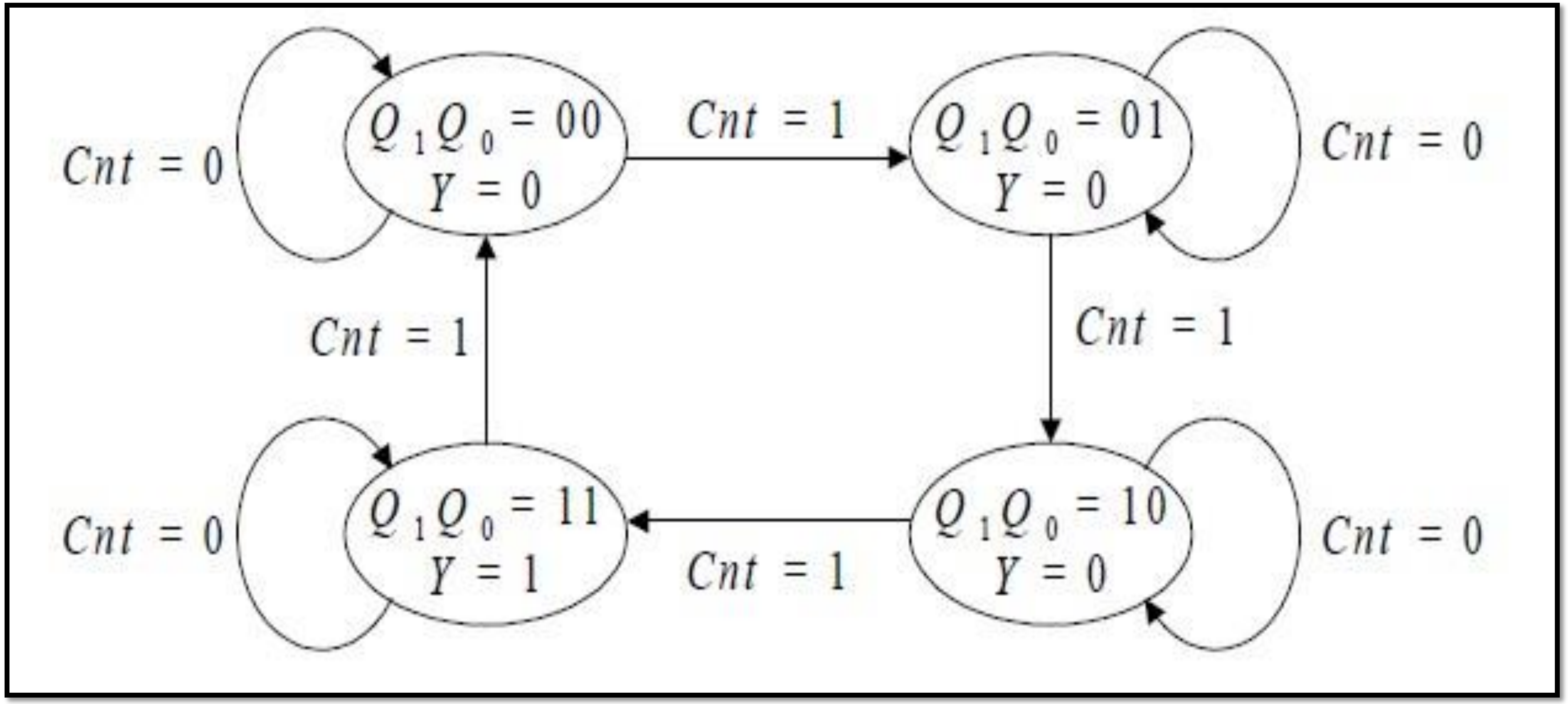
Step 3b:

- Instead of a next-state table, we could use a state diagram to represent the behavior of the sequential circuit.
- A state diagram is basically a pictorial representation of the next-state table. It has exactly one node for each present state in the next-state table.
- As long as Cnt=1, the sequential circuit visits the states in the sequence 0,1,2,3,0,1,2,….
- When Cnt=0, the circuit stays in its present state until Cnt changes to 1, at which point the counting continues.
- We conclude that the circuit is a modulo-4 counter with one control signal, Cnt.

# Moore Machine

Step 3b:

- State diagram

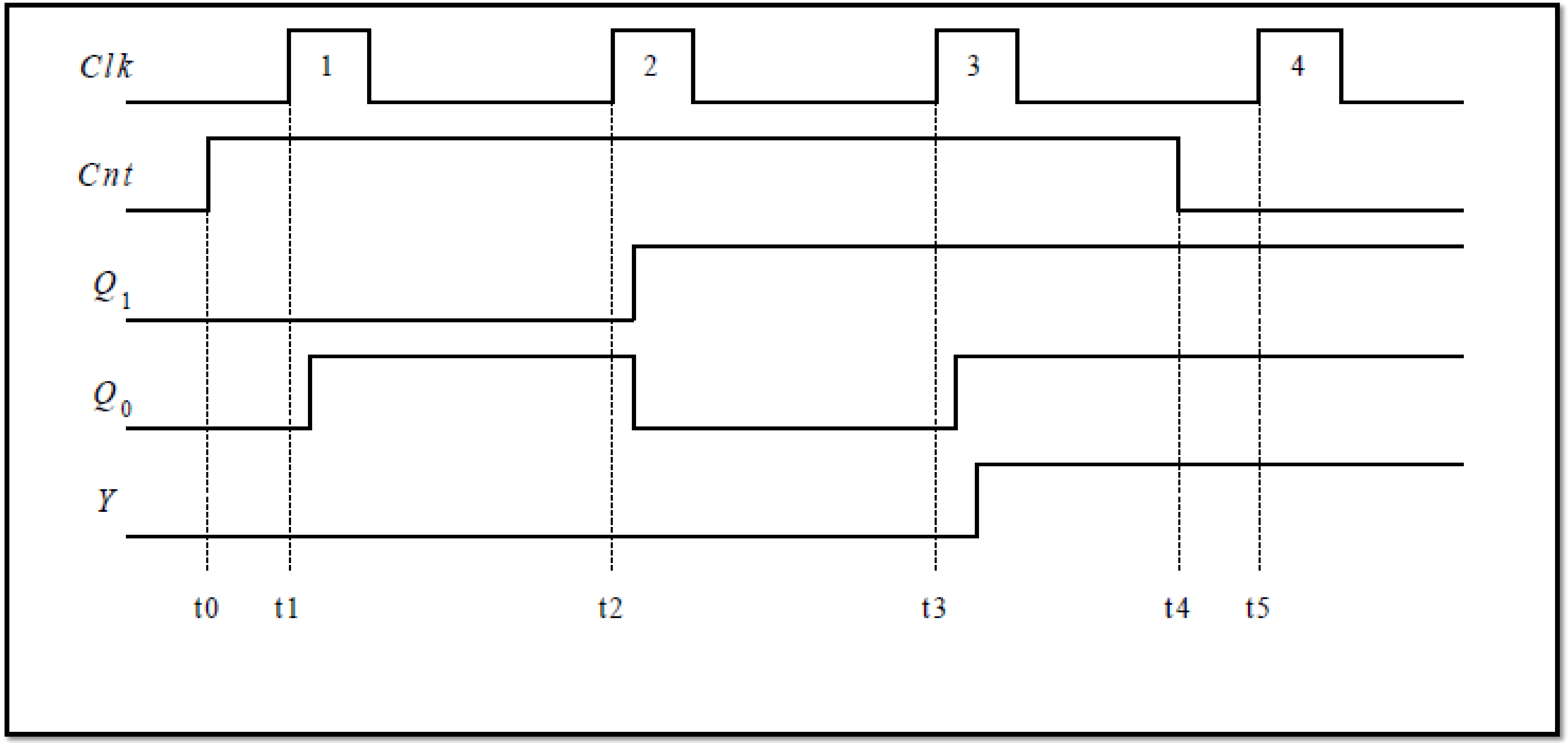


# Moore Machine

**Solution:**

Step 4:

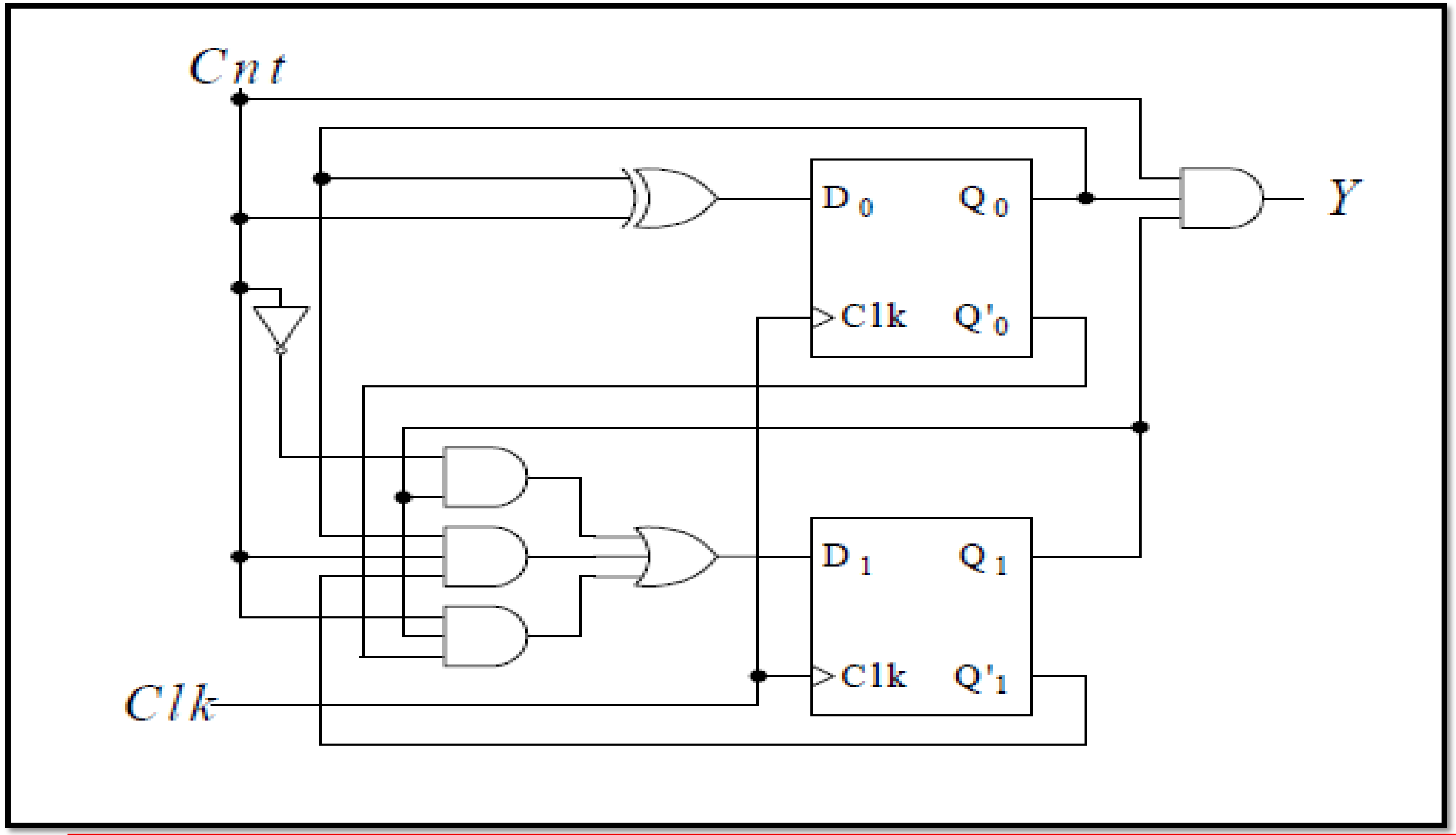
The timing diagram is shown below:



# Mealy Model

**Input-based or Mealy-type sequential circuit.** The output values are dependent on the input values as well as its present state.

Derive the next state, the output tables, and the state diagram for the (modulo-4 counter) sequential circuit represented by the following schematic.



# Mealy Model

**Solution:**

Step 1 (Mealy): Derive excitation equations.

$$D_0 = Cnt \oplus Q_0 = Cnt'Q_0 + CntQ_0'$$
$$D_1 = Cnt'Q_1 + CntQ_1'Q_0 + CntQ_1Q_0'$$

Step 2a (Mealy): Derive the next-state equations.

$$Q_{0next} = D_0 = Cnt \oplus Q_0 = Cnt'Q_0 + CntQ_0'$$
$$Q_{1next} = D_1 = Cnt'Q_1 + CntQ_1'Q_0 + CntQ_1Q_0'$$

Step 2b (Mealy): Derive the output equation.

$$Y = CntQ_1Q_0$$

# Mealy Model

**Solution:**

Step 3a (Mealy):

Derive the next-state/output table. Every entry in the next-state table will represent the next-state and the output value, separated by a slash (/).

| Present State | Next State / Outputs | |
|---|---|---|
| $Q_1Q_0$ | $Q_{1\,next}\,Q_{0\,next}\,/\,Y$ | |
| | $Cnt = 0$ | $Cnt = 1$ |
| 00 | 00 / 0 | 01 / 0 |
| 01 | 01 / 0 | 10 / 0 |
| 10 | 10 / 0 | 11 / 0 |
| 11 | 11 / 0 | 00 / 1 |

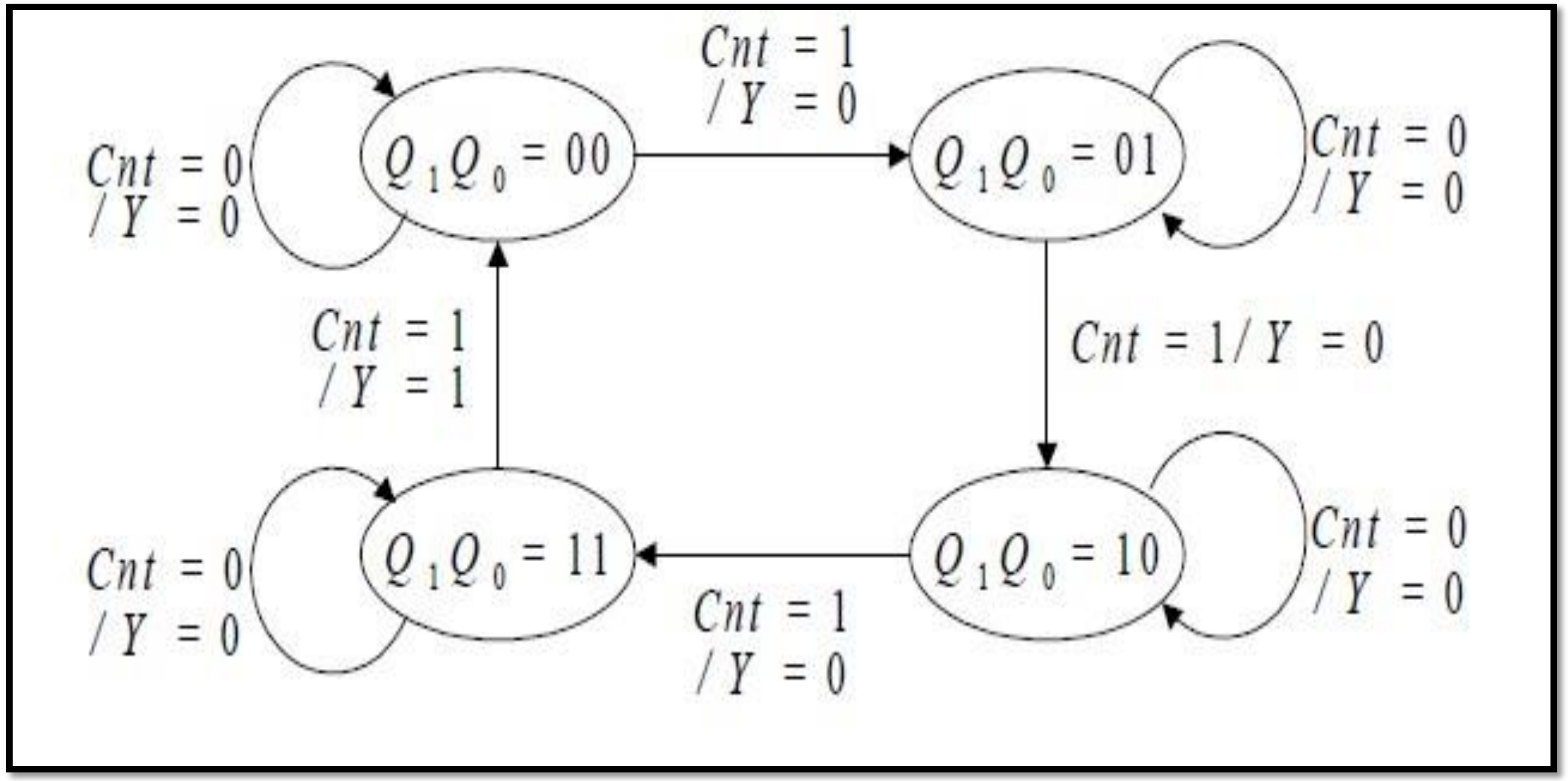
# Mealy Model

**Solution:**

Step 3b (Mealy): Derive the State diagram.

The output is not associated with the state but with the transition arc.

Each arc is labeled with both the input values that move the circuits from the present state to the next state, and the output values, which correspond to the input-signal values in the present state.

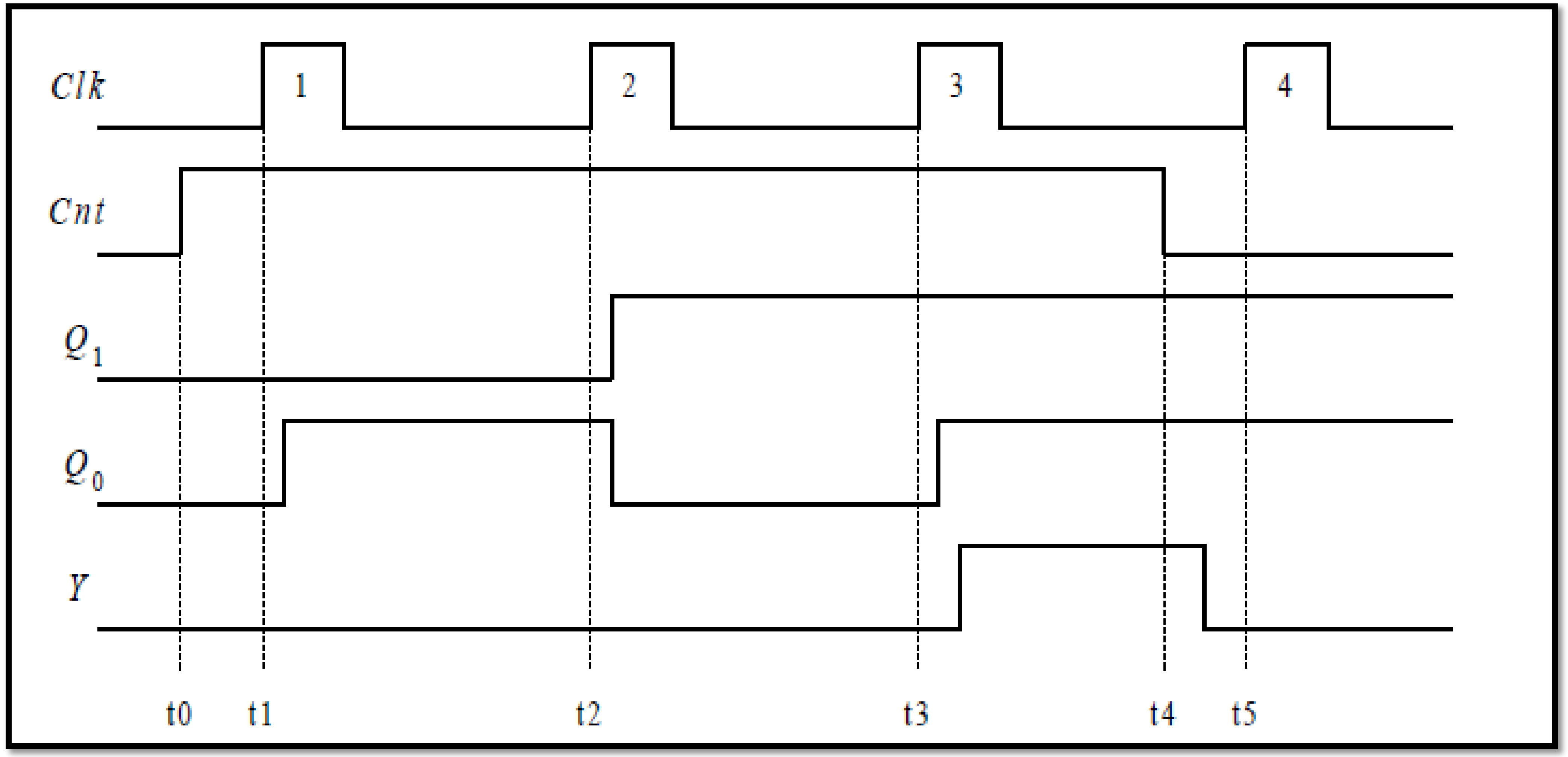


# Mealy Model

**Solution:**

Step 4 (Mealy):The timing diagram is shown below:

In clock cycle 3, the counter will be in state Q1Q0 = 11 and the output signal Y = 1.
At t4, Y = 0 because the input signal Cnt = 0 even though the counter is still in state Q1Q0 = 11.



# THANK YOU