SHIFT REGISTERS

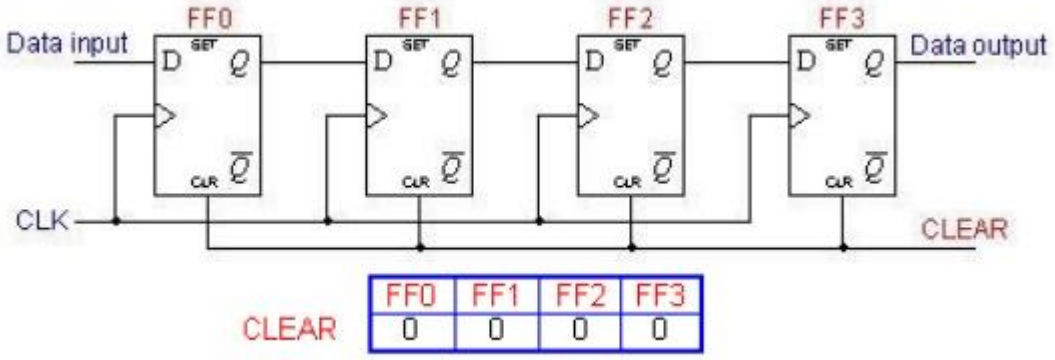
Introduction

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states. All the flip-flops are driven by a common clock, and all are set or reset simultaneously.

The basic types of shift registers are such as Serial In - Serial Out, Serial In - Parallel Out, Parallel In - Serial Out, Parallel In - Parallel Out, and bidirectional shift registers.

1.Serial In - Serial Out Shift Registers

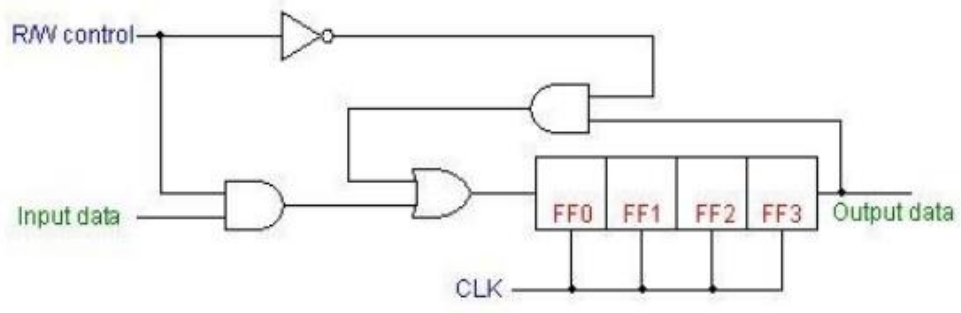
A basic four-bit shift register can be constructed using four D flip-flops, as shown below. The operation of the circuit is as follows. The register is first cleared, forcing all four outputs to zero. The input data is then applied sequentially to the D input of the first flip-flop on the left (FF0). During each clock pulse, one bit is transmitted from left to right. Assume a data word to be 1001. The least significant bit of the data has to be shifted through the register from FF0 to FF3.



	FF0	FF1	FF2	FF3
CLEAR	0	0	0	0

In order to get the data out of the register, they must be shifted out serially. This can be done destructively or non-destructively. For destructive readout, the original data is lost and at the end of the read cycle, all flip-flops are reset to zero.

To avoid the loss of data, an arrangement for a non-destructive reading can be done by adding two AND gates, an OR gate and an inverter to the system. The construction of this circuit is shown below.

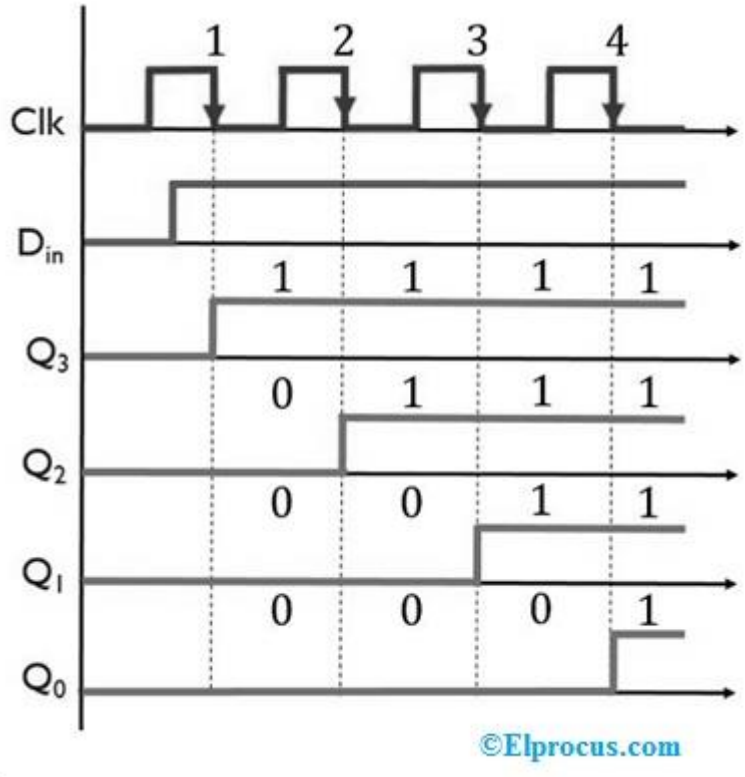


The data is loaded to the register when the control line is HIGH (ie WRITE). The data can be shifted out of the register when the control line is LOW (ie READ).

The **SISO shift register truth table** is shown below.

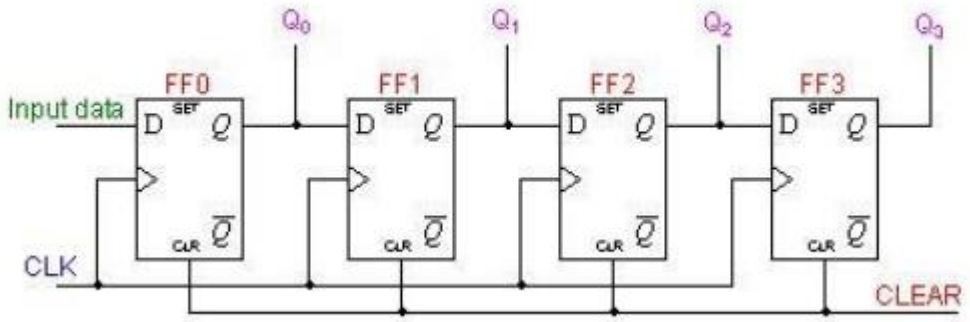
CLK	'Q3'	'Q2'	'Q1'	'Q0'
Initially (Reset)	0	0	0	0
1st Falling Edge	1	0	0	0
2nd Falling Edge	1	1	0	0
3rd Falling Edge	1	1	1	0
4th Falling Edge	1	1	1	1

By considering the above truth table, the SISO shift register waveform representation will be like the following.



2. Serial In - Parallel Out Shift Registers

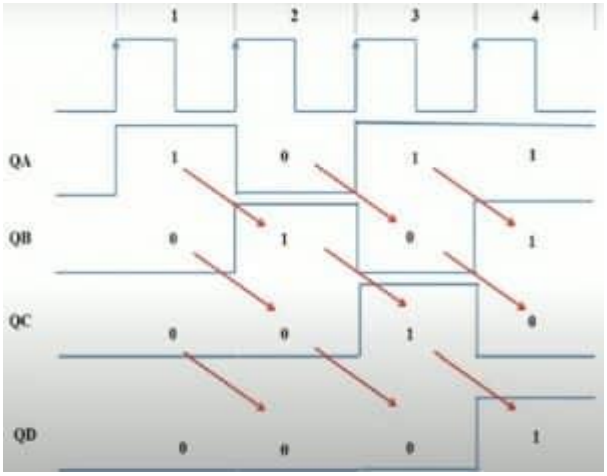
For this kind of register, data bits are entered serially in the same manner as discussed in the last section. The difference is the way in which the data bits are taken out of the register. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously. A construction of a four-bit serial in - parallel out register is shown below.



The truth table for SIPO is

CLK Pulse	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	0	1	0
4	1	1	0	1

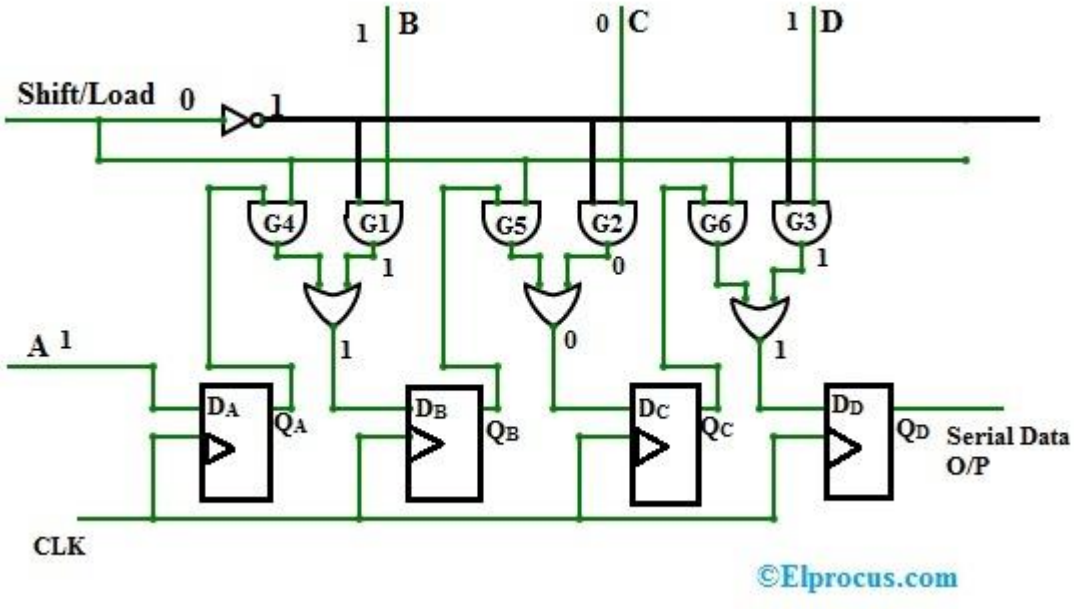
The timing diagram for SIPO is



Here we are using a positive edge CLK i/p signal. In a first clock pulse the input data becomes QA = '1' and all other values like QB, QC, and QD become '0'. So the output will become '1000'. In the second clock pulse, the output will become '0101'. In the third clock pulse, the output will become '1010' and in the fourth clock pulse, the output will become '1101'

3. Parallel In - Serial Out Shift Registers

A four-bit parallel in - serial out shift register is shown below. The circuit uses D flip-flops and NAND gates for entering data (ie writing) to the register.



The PISO shift register truth table is shown below.

Now the control signal applied is '0' then the data to be loaded and the data will become 1101.

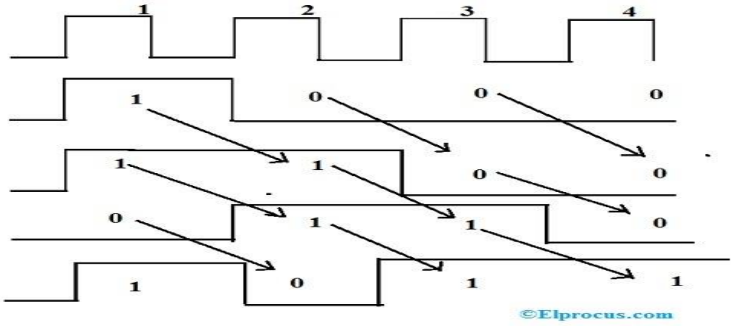
D_A	D_B	D_C	D_D
1	1	0	1

Now the control signal applied is '1' and the CLK pulse '1' is applied then the data is shifted like Q_A becomes '1', Q_B becomes '1', Q_C becomes '0' and Q_D becomes '1' as shown in the following table.

CLK Pulse	Q_A	Q_B	Q_c	Q_D (Data Output)
0	0	0	0	0

1	1	1	0	1
2	0	1	1	0
3	0	0	1	1
4	0	0	0	1

If the CLK pulse ‘2’ is applied then the data is shifted like Q_A becomes ‘0’, Q_B becomes ‘1’, Q_C becomes ‘1’ and Q_D becomes ‘0’ as shown in the following table.
If the CLK pulse ‘3’ is applied then the data is shifted like Q_A becomes ‘0’, Q_B becomes ‘0’, Q_C becomes ‘1’ and Q_D becomes ‘1’ as shown in the following table.
If the CLK pulse ‘4’ is applied then the data is shifted like Q_A becomes ‘0’, Q_B becomes ‘0’, Q_C becomes ‘0’ and Q_D becomes ‘1’ as shown in the following table.

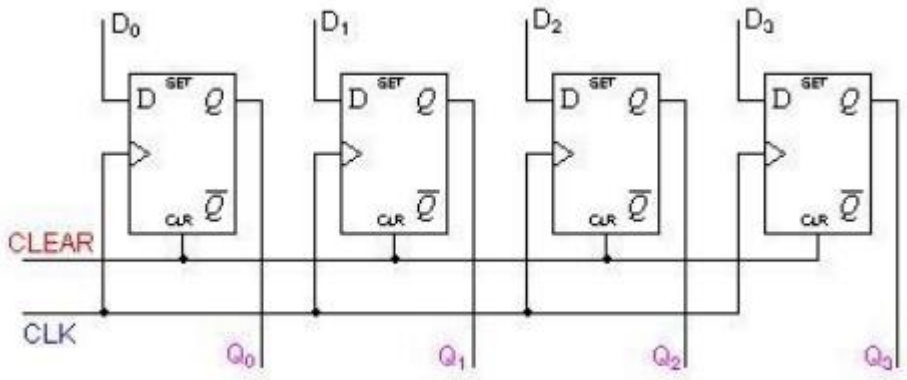


D0, D1, D2 and D3 are the parallel inputs, where D0 is the most significant bit and D3 is the least significant bit. To write data in, the mode control line is taken to LOW and the data is clocked in. The data can be shifted when the mode control line is HIGH as SHIFT is active high. The register performs right shift operation on the application of a clock pulse.

4. Parallel In - Parallel Out Shift Registers

For parallel in - parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit parallel in - parallel out shift register constructed by D flip-flops.

The D's are the parallel inputs and the Q's are the parallel outputs. Once the register is clocked, all the data at the D inputs appear at the corresponding Q outputs simultaneously

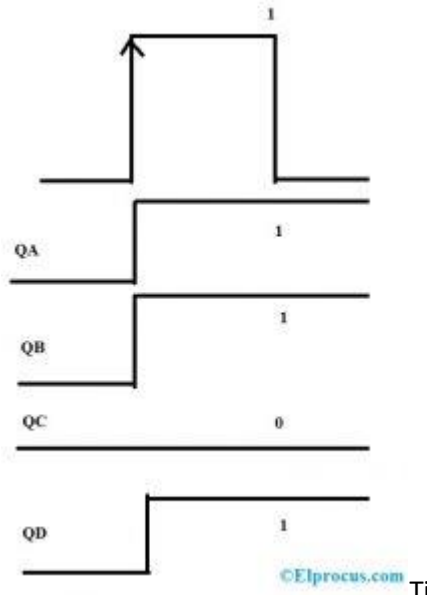


The **truth table of the PIPO shift register** is shown below.

CLK Pulse	QA	QB	QC	QD
0	0	0	0	0
1	1	1	0	1

Timing Diagram

The PIPO shift register timing diagram is shown below. Here we are using positive edge clock input. If we use a positive edge CLK pulse, at that time the transition can take place. So the input data is to be shifted to output, so QA is '1', QB is '1', QC is '0' and QD is '0'. This is the output data.



Timing Diagram

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