SNS COLLEGE OF TECHNOLOGY

Coimbatore-35

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF COMPUTER SCIENCE ENGINEERING

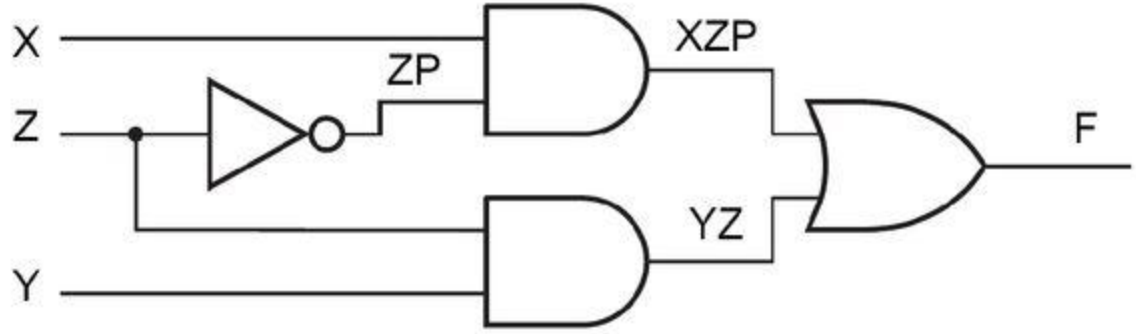
19ECB231 – DIGITAL ELECTRONICS

II YEAR/ III SEMESTER

UNIT 4 – DESIGN OF SEQUENTIAL CIRCUITS

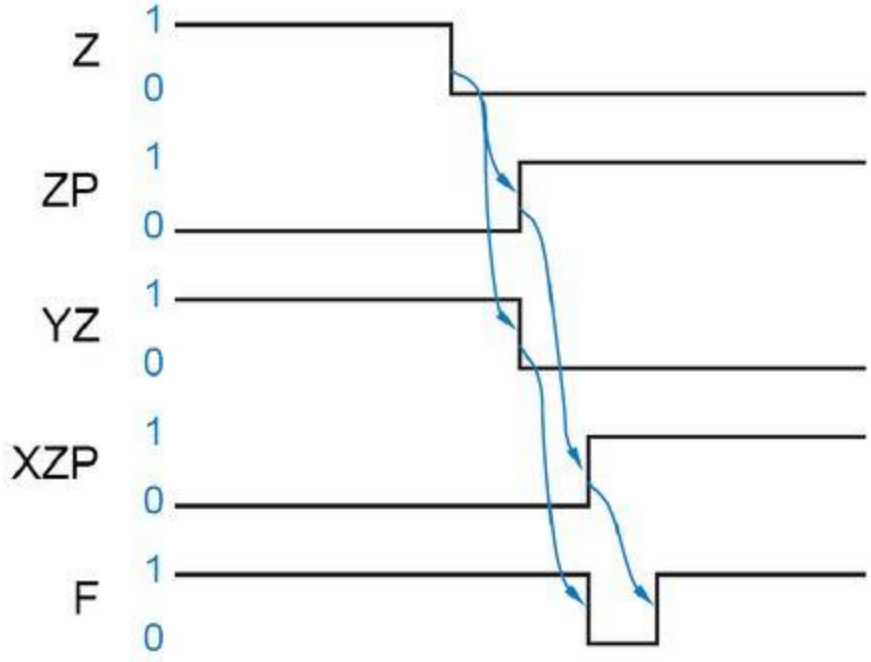
TOPIC –HAZARDS

HAZARDS



Initially:

X=Y=Z=1



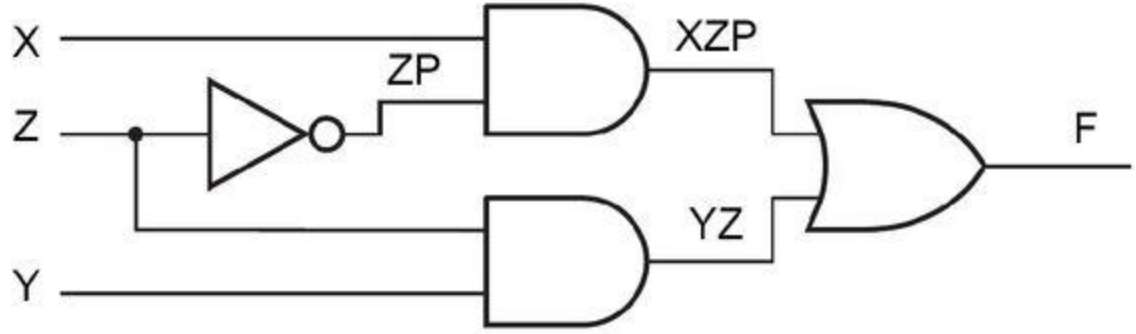
Static Hazard

- **Definition:**
  - A static-1 hazard is the possibility of a 0 glitch when we expect the output to remain at a nice steady 1 based on a static analysis
- **Formal Definition:**
  - A static-1 hazard is a pair of input combinations that:

    (a) differ in only one input variable and

    (b) both give a 1 output;

    such that it is possible for a momentary 0 output to occur during a transition in the differing input variable.



- Even though "static" analysis predicts that the output is 1 for both input combinations

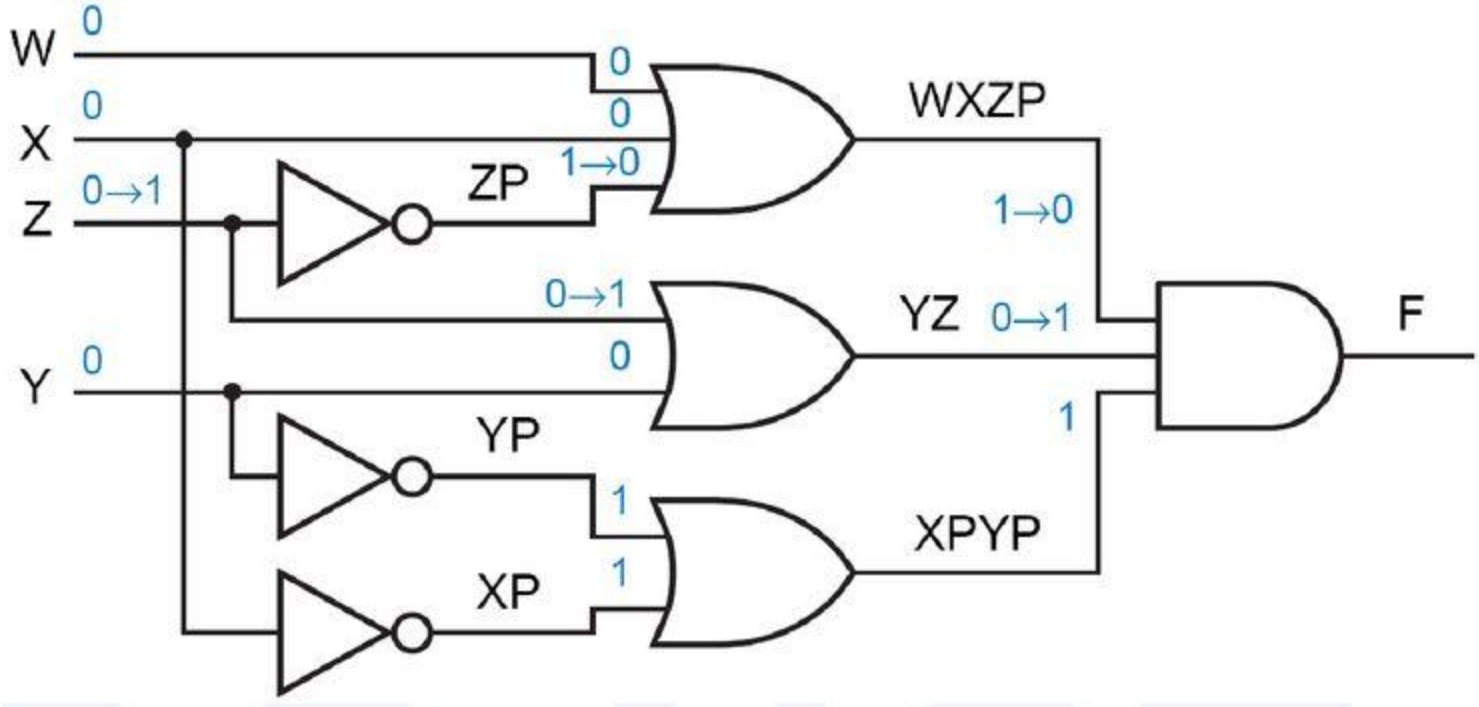
  X,Y,Z = 111 and X,Y,Z = 110,

F goes to 0 for one unit time.

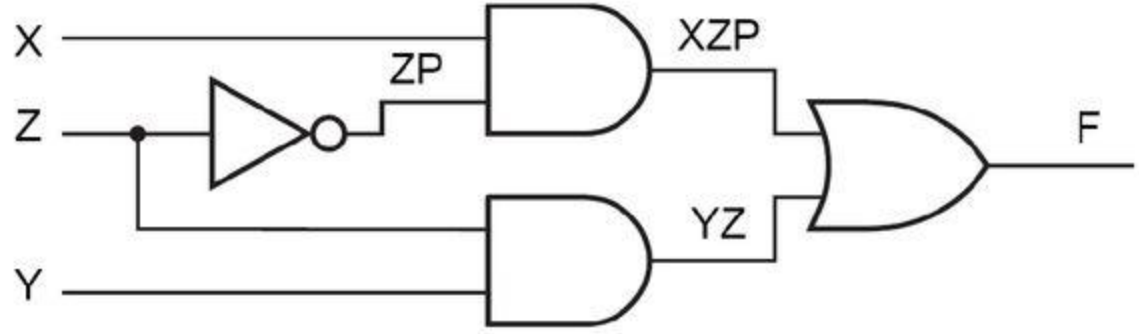
Static-0 Hazard

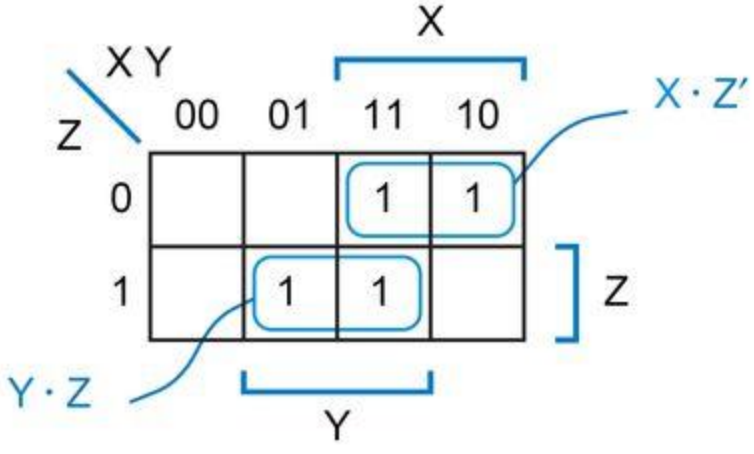
- A properly designed **two-level sum-of-products** (AND-OR) circuit has no static-0 hazards.
- A static-0 hazard is just the **dual** of a static-1 hazard
  - → an **OR-AND circuit** that is the dual of the example circuit would have a static-0 hazard.

- تحلیل کنید:

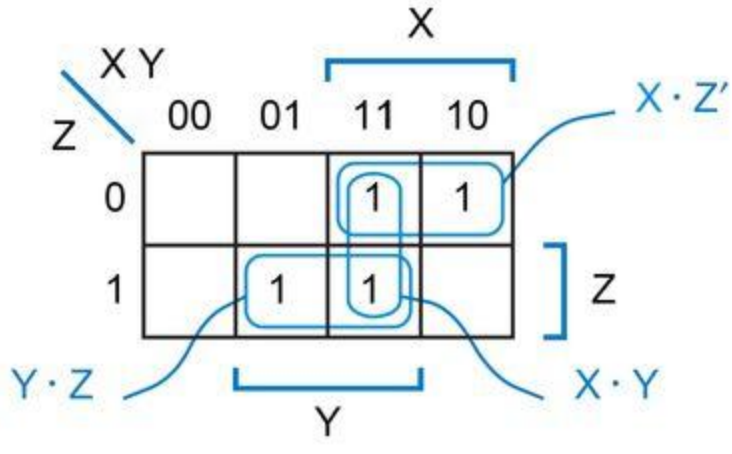


A **Karnaugh map** can be used to detect static hazards in a two-level SOP or POS circuit.

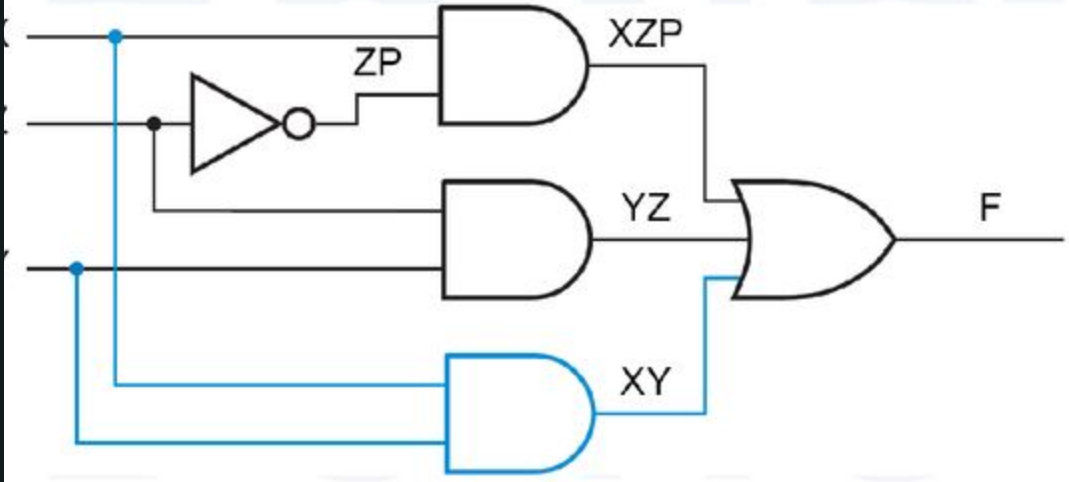


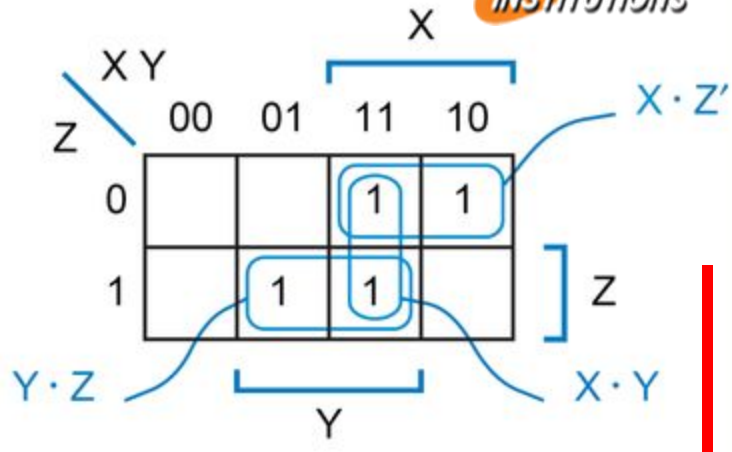


$F = X \cdot Z' + Y \cdot Z$

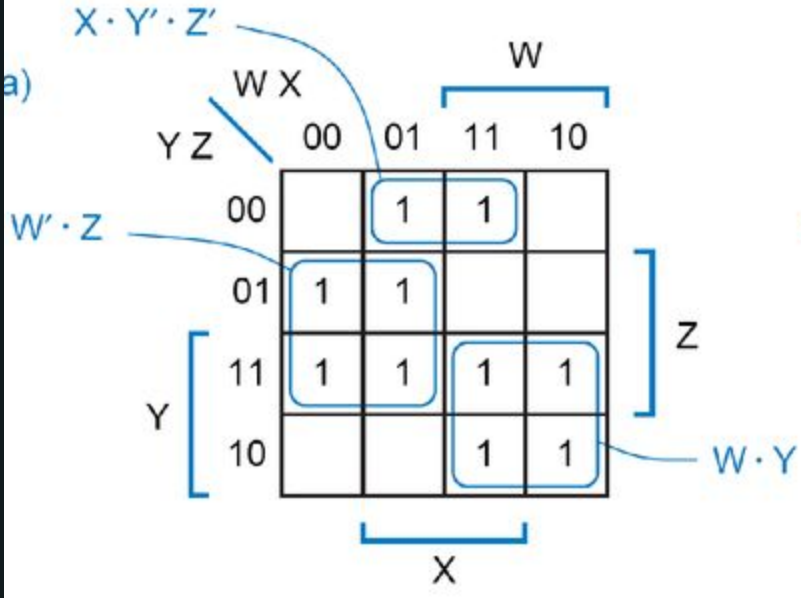


$F = X \cdot Z' + Y \cdot Z + X \cdot Y$

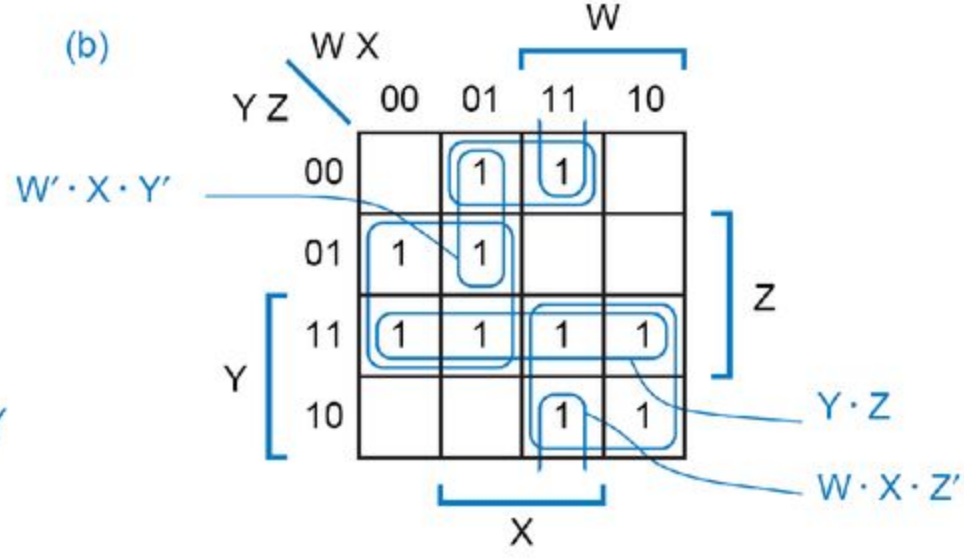




$$F = X \cdot Z' + Y \cdot Z + X \cdot Y$$



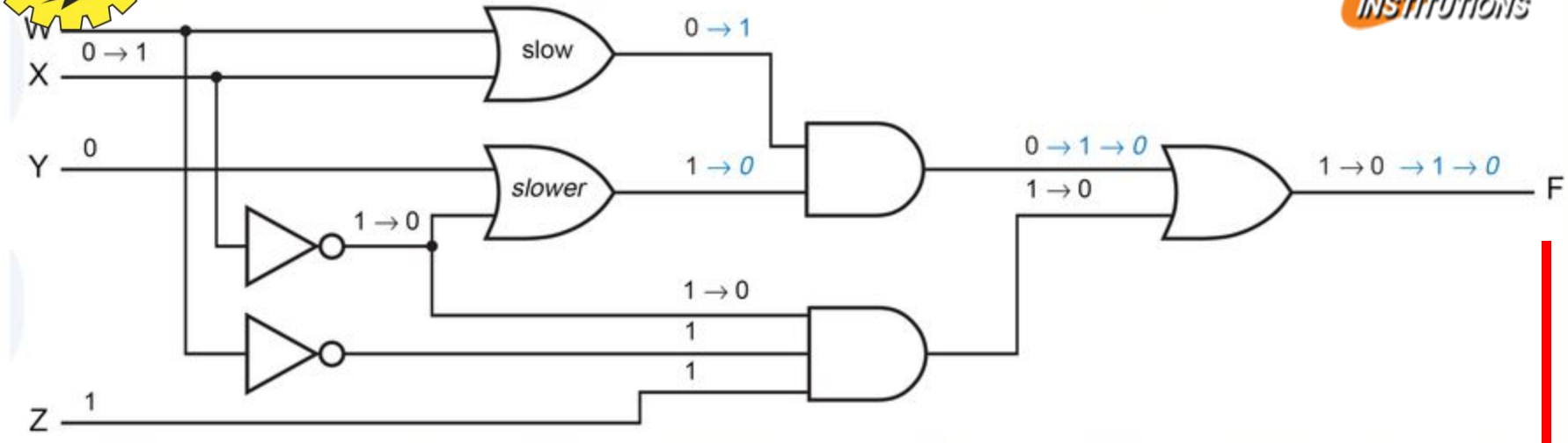
$F = X \cdot Y' \cdot Z' + W' \cdot Z + W \cdot Y$



$F = X \cdot Y' \cdot Z' + W' \cdot Z + W \cdot Y + W \cdot X \cdot Y' + Y \cdot Z' + W \cdot X \cdot Z'$

Dynamic Hazard

- **Dynamic hazard:**
  - the possibility of an output changing **more than once** as the result of a single input transition.
    - Multiple output transitions can occur if there are **multiple paths with different delays** from the changing input to the changing output.


W
X
Y
Z
0 → 1
0
1
slow
slower
0 → 1
1 → 0
1 → 0
1 → 0
1
1
0 → 1 → 0
1 → 0
1 → 0 → 1 → 0
F

- Techniques for finding hazards in arbitrary circuits, are rather difficult to use.
  - → when you require a hazard-free design, it's best to use a circuit structure that is easy to analyze.
- In particular, two-level AND-OR circuit has no static-0 or dynamic hazards.
- Static-1 hazards may exist in such a circuit but they can be found and eliminated using K-map.

- **Most Hazards are not hazardous:**
  - A well-designed, *synchronous* digital system is structured so that hazard analysis is not needed for most of its circuits.
  - In a synchronous system, all of the inputs to a combinational circuit are changed at a particular time, and the outputs are not "looked at" until they have had time to settle to a steady-state value.
  - Hazard analysis and elimination are typically needed only in the design of asynchronous sequential circuits,
  - Asynchronous circuits are not the mainstream but if you want to design them, an understanding of hazards will be absolutely essential for a reliable result.

THANK YOU