SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB231 DIGITAL ELECTRONICS

II YEAR/ III SEMESTER

UNIT-IV DESIGN OF SEQUENTIAL CIRCUITS

DESIGN OF SYNCHRONOUS SEQUENTIAL CIRCUITS: STATE DIAGRAM, STATE TABLE

DESIGN OF SYNCHRONOUS SEQUENTIAL CIRCUITS: STATE DIAGRAM, STATE TABLE

Objectives

1. Design of synchronous sequential circuits with an example.
2. Construction of state diagrams and state tables
3. Translation of State transition table into excitation table.
4. Logic diagram construction of a synchronous sequential circuit

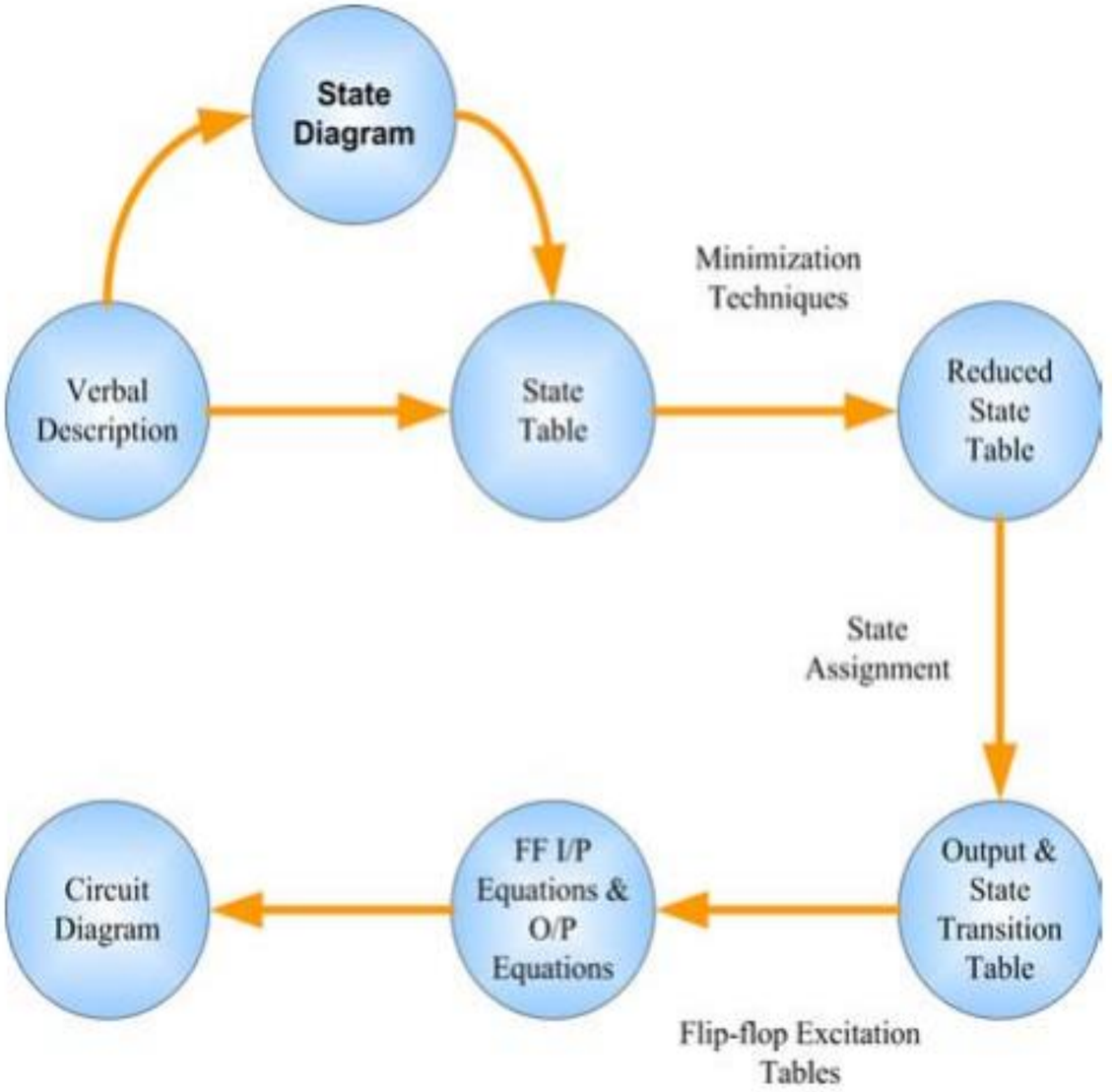


Figure 1: Sequential Circuit Design Steps

DESIGN OF SYNCHRONOUS SEQUENTIAL CIRCUITS: STATE DIAGRAM, STATE TABLE

- The next step is to derive the state table of the sequential circuit. A state table represents the verbal specifications in a tabular form.
- In certain cases state table can be derived directly from verbal description of the problem.
- In other cases, it is easier to first obtain a state diagram from the verbal description and then obtain the state table from the state diagram.
- A state diagram is a graphical representation of the sequential circuit.
- In the next step, we proceed by simplifying the state table by minimizing the number of states and obtain a reduced state table.

DESIGN OF SYNCHRONOUS SEQUENTIAL CIRCUITS: STATE DIAGRAM, STATE TABLE

- The states in the reduced state table are then assigned binary-codes. The resulting table is called output and state transition table.
- From the state transition table and using flip-flop's excitation tables, flip-flops input equations are derived. Furthermore, the output equations can readily be derived as well.
- Finally, the logic diagram of the sequential circuit is constructed.
- An example will be used to illustrate all these concepts.

Sequence Recognizer

- A sequence recognizer is to be designed to detect an input sequence of '1011'. The sequence recognizer outputs a '1' on the detection of this input sequence. The sequential circuit is to be designed using JK and D type flip-flops.

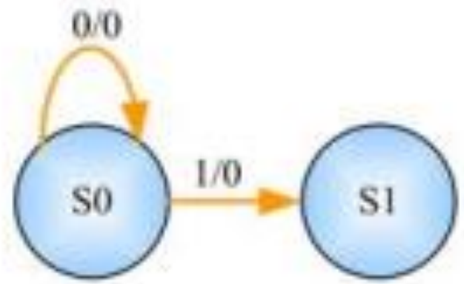
- A sample input/output trace for the sequence detector is shown in Table 1

Table 1: Sample Input/Output Trace

Input	0	1	1	0	1	0	1	1	0	1	1	1	0	1	0	1	1	1	0	0
Output	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0

Deriving the State Diagram

(a)



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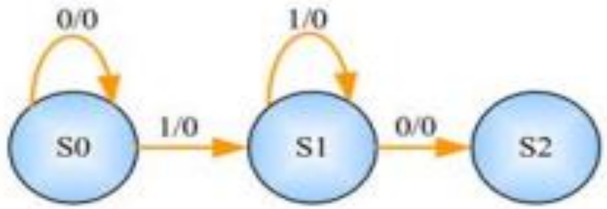

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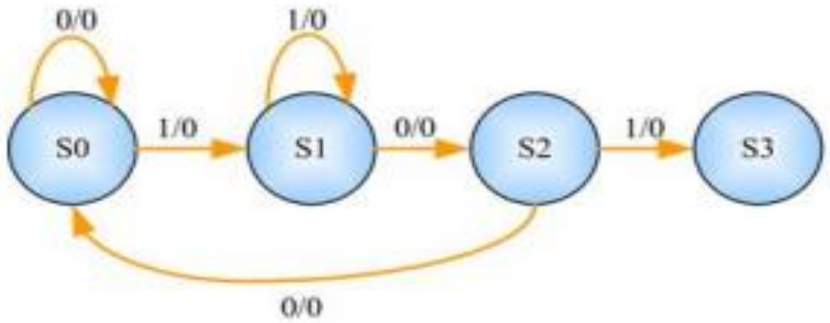

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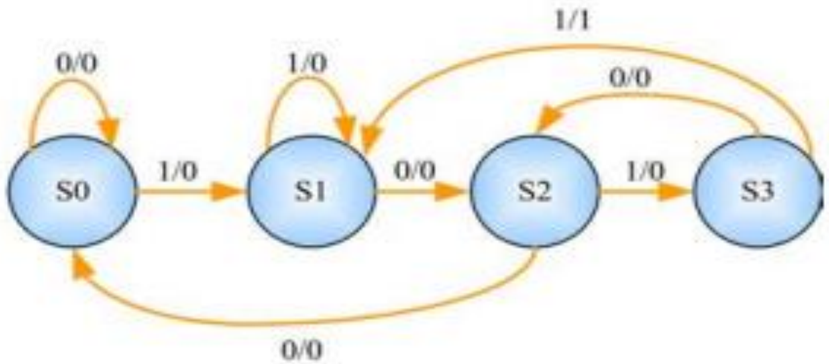

(e)

Figure 2: Deriving the State Diagram of the Sequence Recognizer

Deriving the State Table

Table 2: State Table of the Sequence Recognizer

Present State	Next State		Output	
	X=0	X=1	X=0	X=1
S0	*S0*	*S1*	0	0
S1	*S2*	*S1*	0	0
S2	*S0*	*S3*	0	0
S3	*S2*	*S1*	0	1

State Assignment

Table 4: State Assignment

State	*Assignment*
S0	00
S1	01
S2	10
S3	11

State Assignment

Table 5: State Transition Table

Inputs of Combinational Circuit		Next State	Output
Present State	Input		
A B	*X*	*A B*	*Y*
0 0	0	0 0	0
0 0	1	0 1	0
0 1	0	1 0	0
0 1	1	0 1	0
1 0	0	0 0	0
1 0	1	1 1	0
1 1	0	1 0	0
1 1	1	0 1	1

THANK YOU