SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A+' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB231 DIGITAL ELECTRONICS

II YEAR/ III SEMESTER

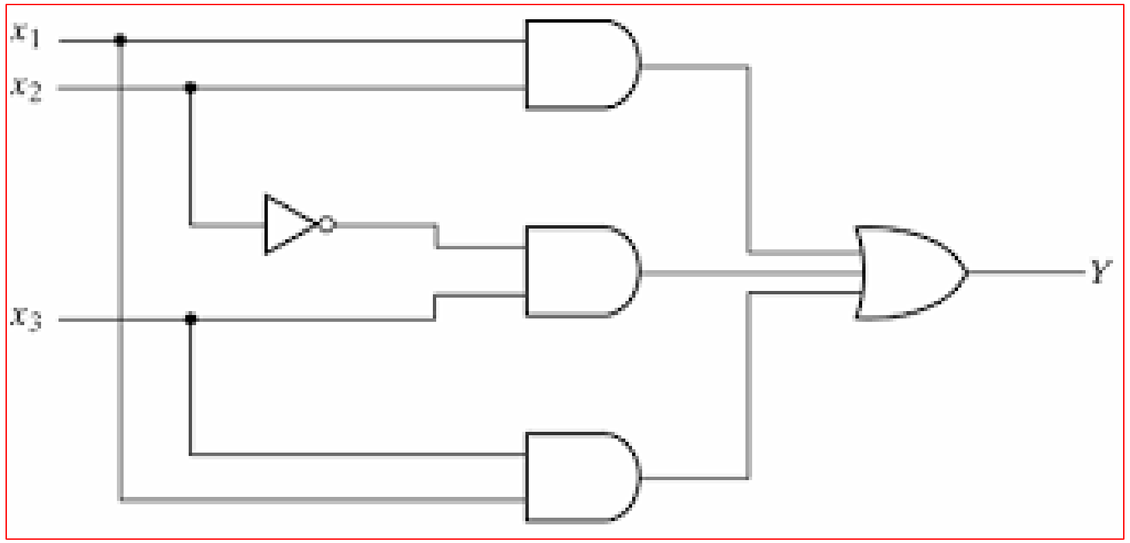
UNIT-IV DESIGN OF SEQUENTIAL CIRCUITS

Topic 9- Introduction to Hazards – Static and Dynamic

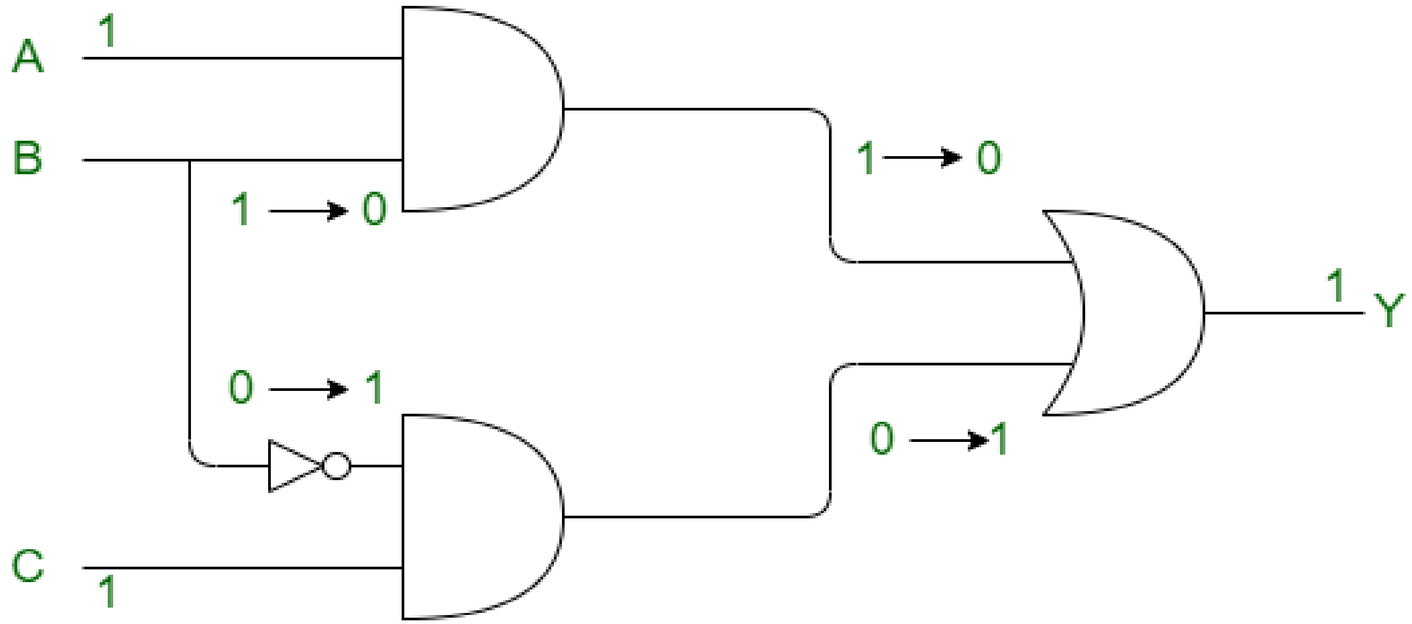
Hazards

•The unwanted switching transient occur in a digital circuit is called hazard.

Eg: Consider a logic circuit, which is expected to give a logic -1 output, momentarily becomes logic o because of finite propagation delays of various gates.



Hazards in Combinational Logic Circuits



AND-OR Circuit containing Static Hazard

Classification of Hazards

Hazards are classified into three types:

1. **Static hazard**
   a) **Static -1 Hazard**
   b) **Static -0 hazard**
2. **Dynamic Hazard**
3. **Essential Hazard**

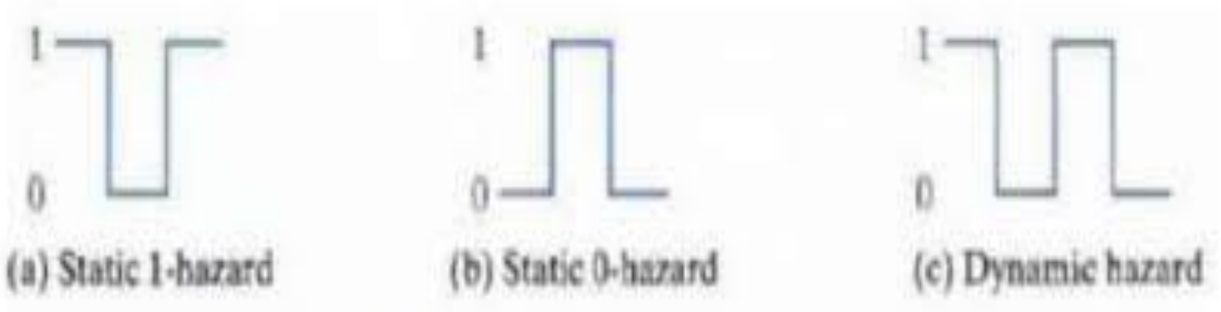
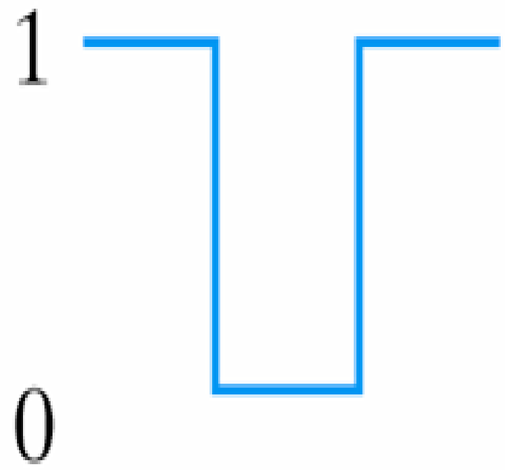


Fig: Types of hazards

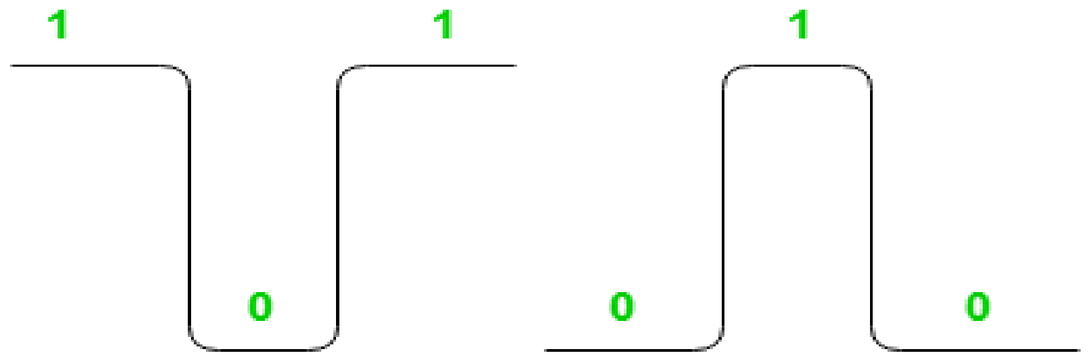
Static – 1 Hazard

In response to an input change and for some combination of propagation delays, a logic circuit may go to 0 when it should remain constant 1, this transient is called static-1 hazard



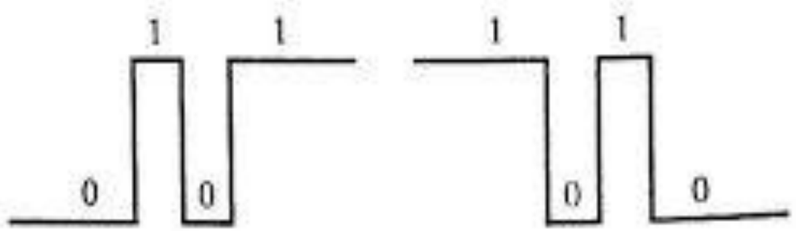
Static -0 Hazard

In response to an input change and for some combination of propagation delays, a logic circuit may go to 1 when it should remain constant at o, this transient is called Static-0 hazard



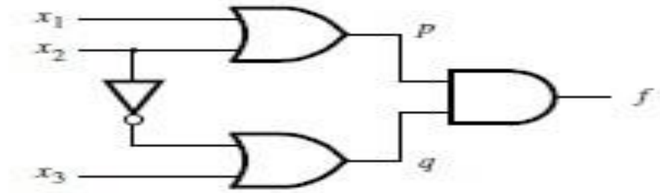
Dynamic Hazard

When the output of logic circuit is changed from 0 to 1 and 1 to 0. These two outputs may change more number of times, this transient is called dynamic hazard.

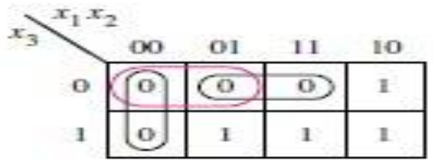


(c) Dynamic hazards

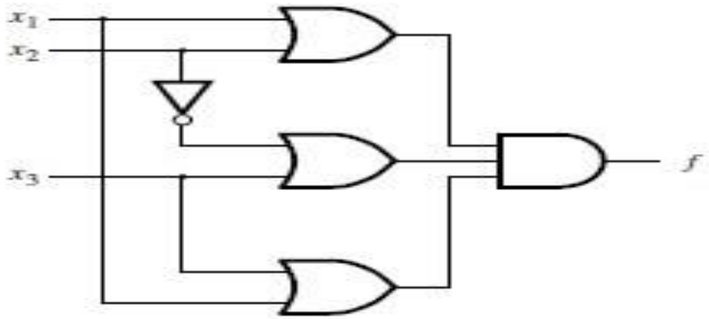
Prevention of Hazards in Logic gates



(a) Circuit with a hazard



(b) Karnaugh map



(c) Hazard-free circuit

Figure 9.65 Static hazard in a POS circuit.

9.6.3 Significance of Hazards

Essential Hazards

The static and dynamic hazards can occur in combinational as well as sequential logic circuits. Essential hazards occur in sequential circuits only

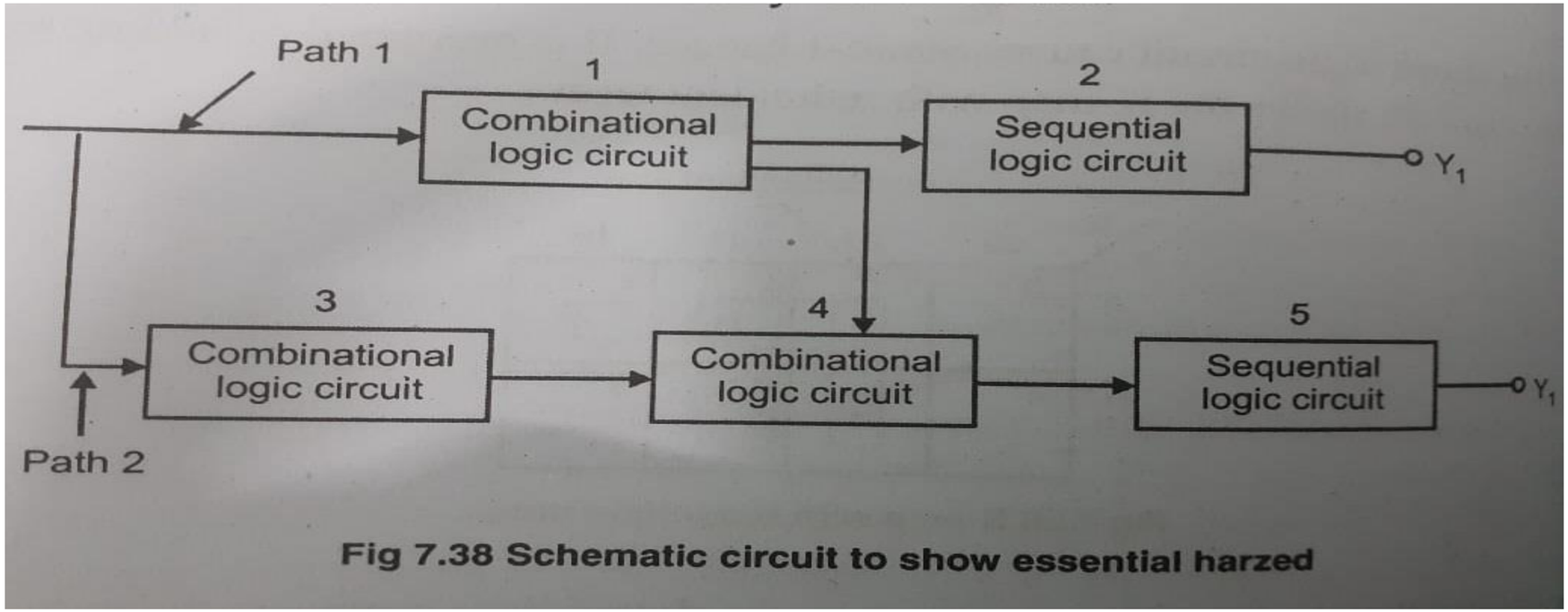


Fig 7.38 Schematic circuit to show essential harzed

THANK YOU