SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

19ECB231 –DIGITAL ELECTRONICS

II YEAR/ III SEMESTER

UNIT 4 –DESIGN OF SEQUENTIAL CIRCUITS

TOPIC –Classification of sequential circuits: Moore and Mealy example

Analysis Procedure

- Identify type of circuit either Mealy or Moore circuit
- Derive excitation equation (Boolean expression)
- Derive next state and output equations
- Generate state table
- Generate state diagram

Analysis Procedure

DESIGN PROCEDURE FOR CLOCKED SEQUENTIAL CIRCUIT

The following steps are followed to design the clocked sequential logic circuit.

•Obtain the state table from the given circuit information such as a state diagram, a timing diagram or description.

•The number of states may be reduced by state reduction technique.

•Assign binary values to each state in the state table.

•Determine the number of flip flops required and assign a letter symbol to each flip flop.

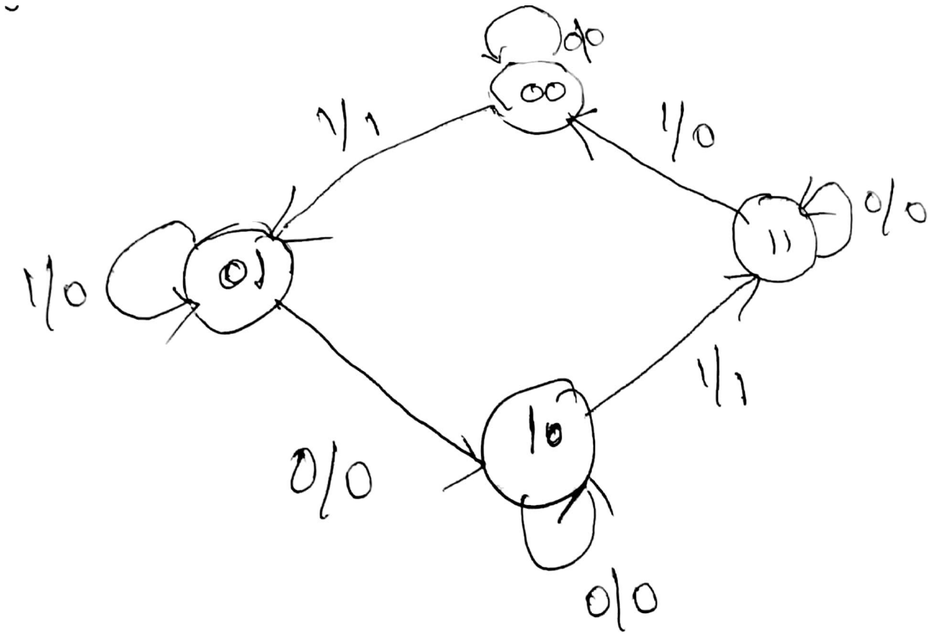
•Choose the flip flop type to be used according to the application.

•Derive the excitation table from the reduced state table.

•Derive the expression for flip flop inputs and outputs using k-map simplification (The present state and inputs are considered for k-map simplification) and draw logic circuit

Mealy Model

Design the synchronous sequential circuit for mealy diagram using D flip flop



Solution

Step 1: State Table

Table 6.15: State Table

Present State		Next State				Output	
		$x=0$		$x=1$		$x=0$	$x=1$
A	B	A	B	A	B	Y	y
0	0	0	0	0	1	0	1
0	1	1	0	0	1	0	0
1	0	1	0	1	1	0	1
1	1	1	1	0	0	0	0

Step 2: Excitation table for design with D flip flops:

Table 6.16 : Excitation table for D flip flop

Present State	Next State	Input
$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

Table 6.17: Excitation table for design with D flip flops

Present State		Input	Next State		Flip Flop Inputs		Output
A	B	x	$A(t+1)$	$B(t+1)$	DA	DB	Y
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	1
0	1	0	1	0	1	0	0
0	1	1	0	1	0	1	0
1	0	0	1	0	1	0	0
1	0	1	1	1	1	1	1
1	1	0	1	1	1	1	0
1	1	1	0	0	0	0	0

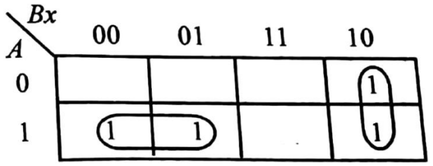
$D = Q(t+1)$

Therefore, $DA = A(t+1)$

$DB = B(t+1)$

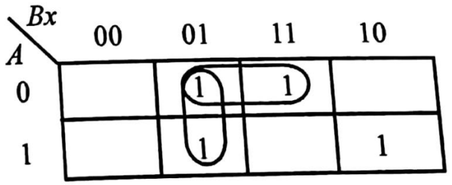
Step 3: K map simplification for flip flop input functions and circuit output function

Expression for DA



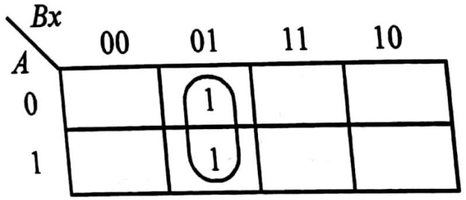
$$DA = A\overline{B} + B\overline{x}$$

Expression for DB



$$DB = \overline{A}x + \overline{B}x + AB\overline{x}$$

Expression for *y*



$$Y = \overline{B}x$$

Step 4: Logic Diagram

The simplified functions are:

$$DA = A\overline{B} + B\overline{x}$$

$$DB = \overline{A}x + B\overline{x} + AB\overline{x}$$

$$Y = \overline{B}x$$

Moore Machine

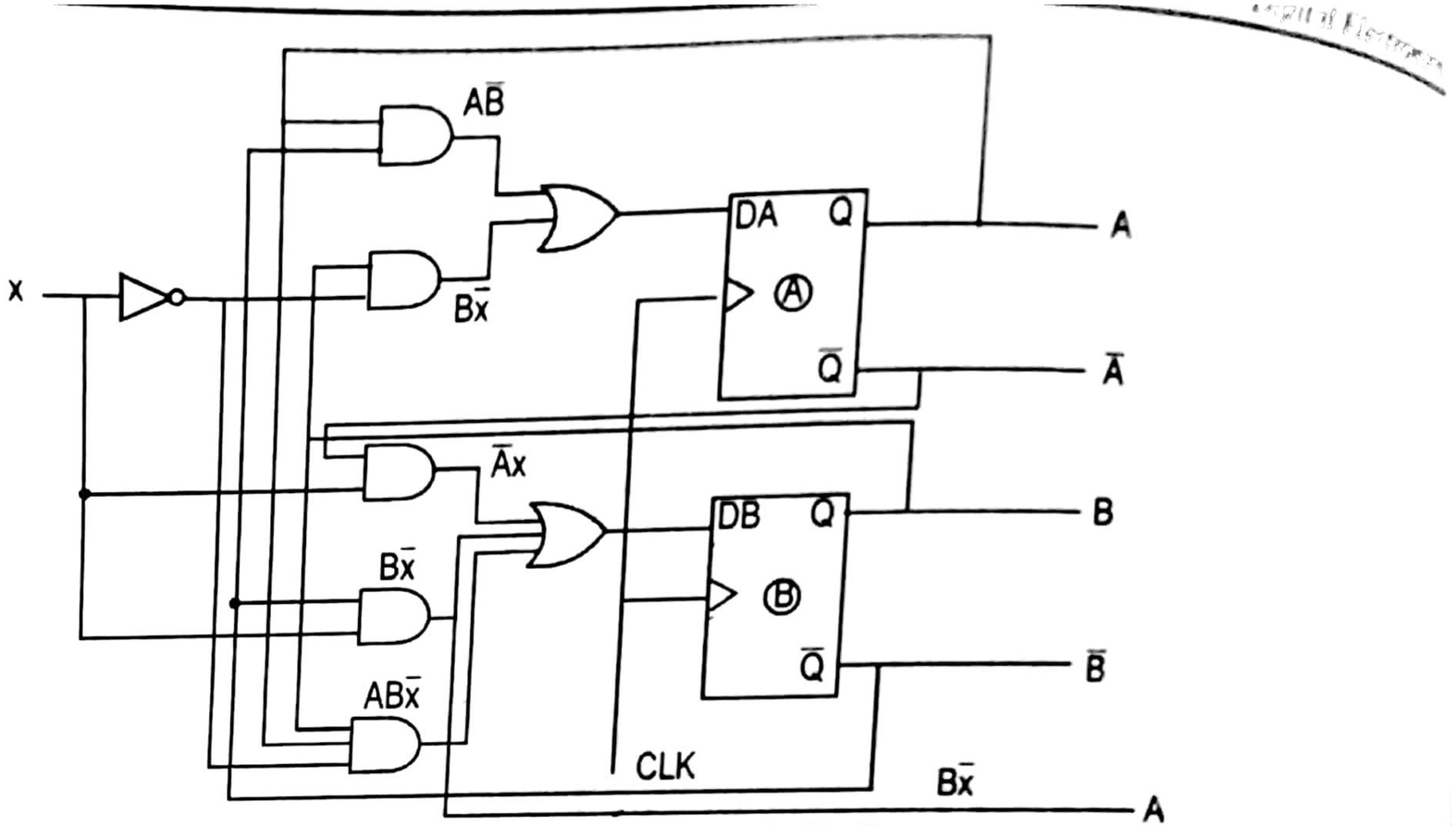


Fig. 6.17 : Logic diagram with D flip flops

Design the synchronous sequential circuit for the Moore state diagram of **Figure 6.18** using T flip flops.

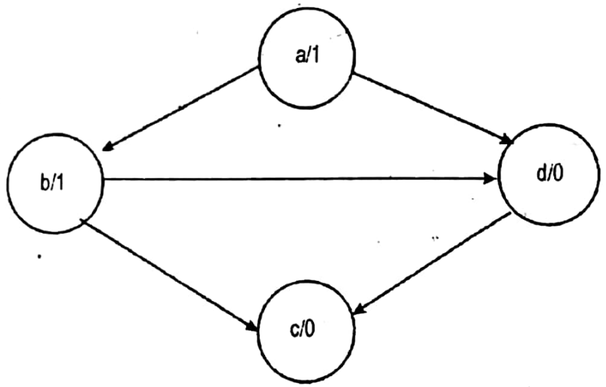


Fig. 6.18 : Moore state diagram

Solution

***Step 1:* State Table:** The state table for the given Moore state diagram is shown in **Table 6.18**.

Table 6.18: State Table

Present State	Next State	Output
a	***b***	**1**
b	c	1
c	d	0
d	a	0

Step 2: Binary Assignment

Assign the binary values 00, 01, 11, 10 to the states a, b, c, d respectively. **Table 6.19** shows the state table with binary assignment.

Table 6.19 : State Table with Binary assignment

Present State		Next State		Output
A	*B*	*A*(*t*+1)	*B*(*t*+1)	*Y*
0	0	0	1	1
0	1	1	1	1
1	1	1	0	0
1	0	0	0	0

Step 3: Excitation table for design with T flip flops.

Table 6.20 shows the excitation table for T flip flop and **Table 6.21** shows the excitation table for given problem.

Table 6.20 : Excitation table for T flip flop

Q(*T*)	*Q*(*t*+1)	*T*
0	0	0
0	1	1
1	0	1
1	1	0

Table 6.21 : Excitation Table

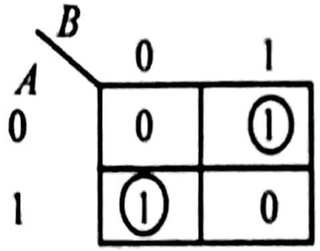
Moore Machine

Table 6.21 : Excitation Table

Present state		Next State		Inputs		Output
A	*B*	*A*(*t*+1)	*B*(*t*+1)	*TA*	*TB*	*Y*
0	0	0	1	0	1	1
0	1	1	1	1	0	1
1	1	1	0	0	1	0
1	0	0	0	1	0	0

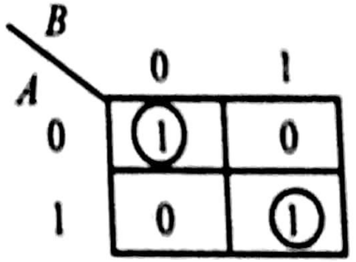
Step 4: K-map simplification for flip flop input functions (*TA, TB*) and output function (*Y*).

Expression for *TA*



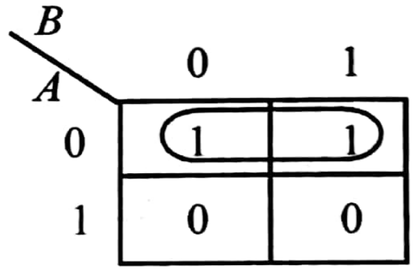
$$TA = \bar{A}B + A\bar{B} = A \oplus B$$

Expression for *TB*



$$TB = \bar{A}\bar{B} + AB = \overline{A \oplus B}$$

Expression for Y



$$Y = \overline{A}$$

Step 5: Logic diagram of Moore sequential circuit with T flip flops.

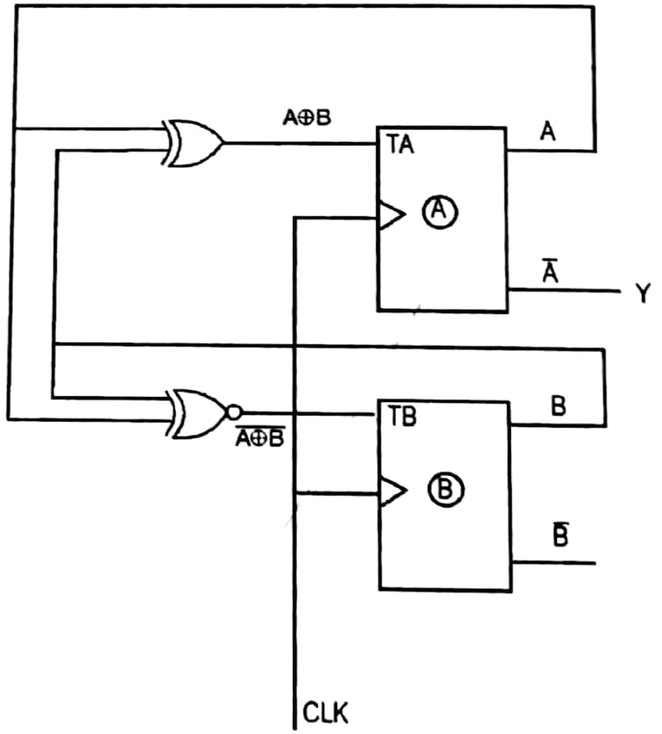
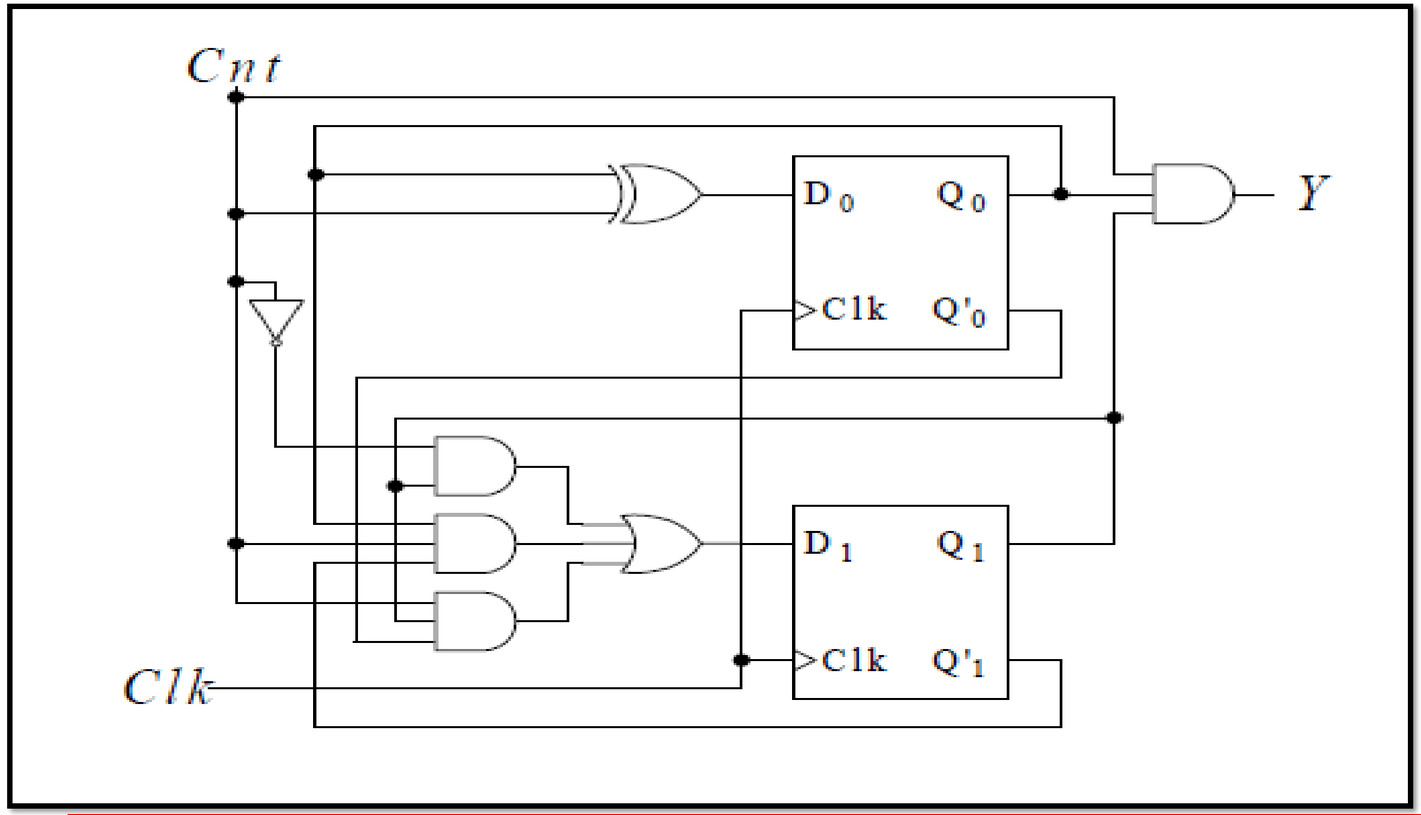


Fig. 6.19 : Moore sequential circuit with T flip flops

Mealy Model

Input-based or Mealy-type sequential circuit. The output values are dependent on the input values as well as its present state.

Derive the next state, the output tables, and the state diagram for the (modulo-4 counter) sequential circuit represented by the following schematic.



Mealy Model

Solution:

Step 1 (Mealy): Derive excitation equations.

$$D_0 = Cnt \oplus Q_0 = Cnt'Q_0 + CntQ_0'$$
$$D_1 = Cnt'Q_1 + CntQ_1'Q_0 + CntQ_1Q_0'$$

Step 2a (Mealy): Derive the next-state equations.

$$Q_{0next} = D_0 = Cnt \oplus Q_0 = Cnt'Q_0 + CntQ_0'$$
$$Q_{1next} = D_1 = Cnt'Q_1 + CntQ_1'Q_0 + CntQ_1Q_0'$$

Step 2b (Mealy): Derive the output equation.

$$Y = CntQ_1Q_0$$

Mealy Model

Solution:

Step 3a (Mealy):

Derive the next-state/output table. Every entry in the next-state table will represent the next-state and the output value, separated by a slash (/).

Present State	Next State / Outputs	
Q_1Q_0	$Q_{1\,next}Q_{0\,next}$ / Y	
	$Cnt = 0$	$Cnt = 1$
00	00 / 0	01 / 0
01	01 / 0	10 / 0
10	10 / 0	11 / 0
11	11 / 0	00 / 1

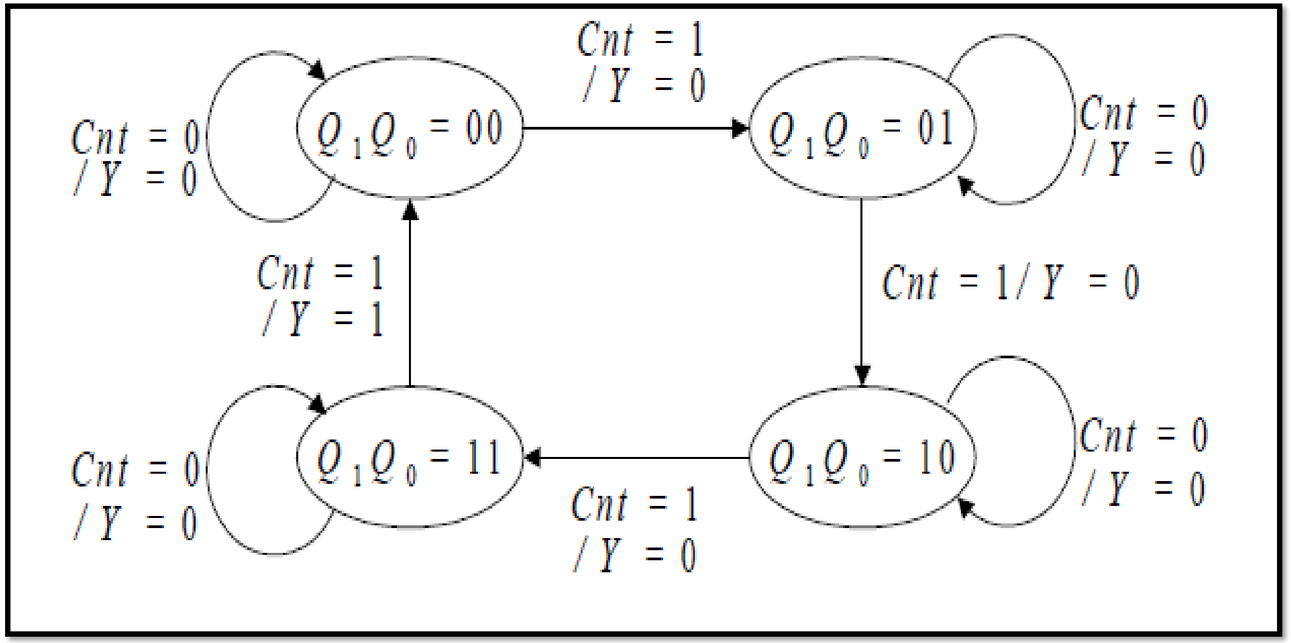
Mealy Model

Solution:

Step 3b (Mealy): Derive the State diagram.

The output is not associated with the state but with the transition arc.

Each arc is labeled with both the input values that move the circuits from the present state to the next state, and the output values, which correspond to the input-signal values in the present state.

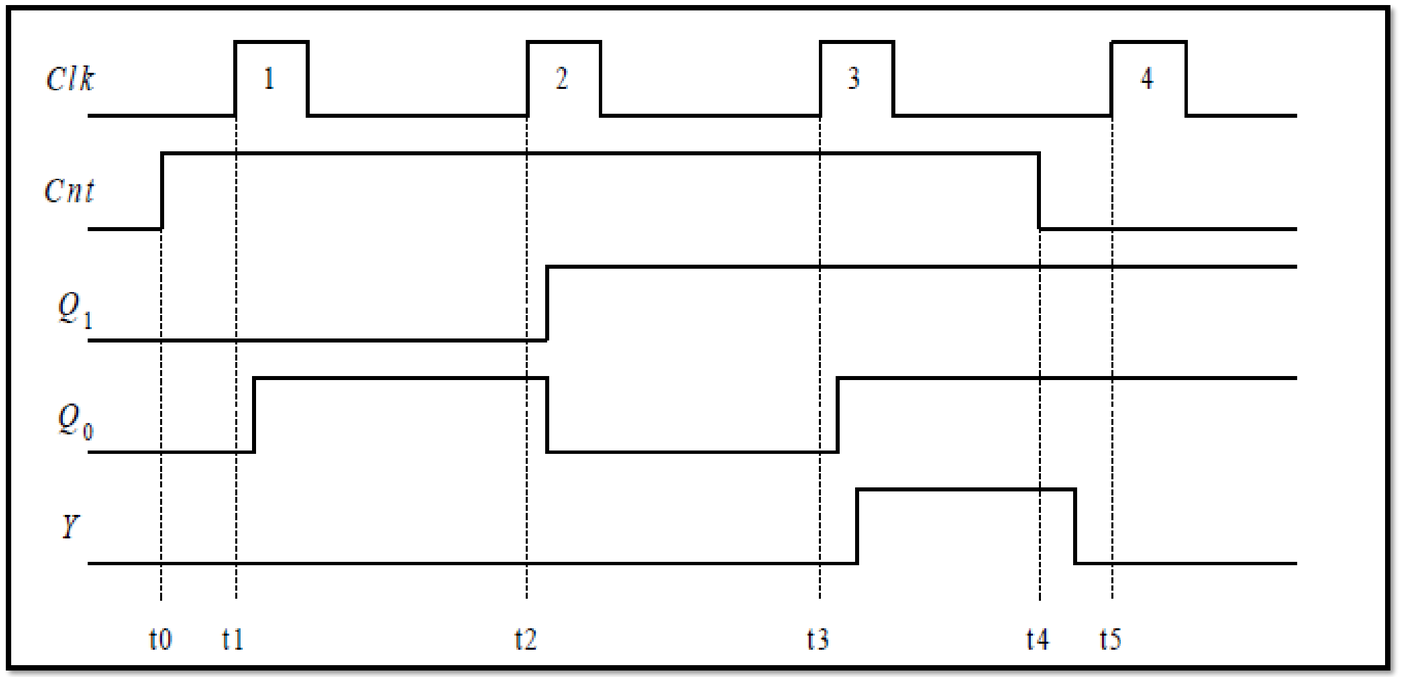


Mealy Model

Solution:

Step 4 (Mealy):The timing diagram is shown below:

In clock cycle 3, the counter will be in state Q1Q0 = 11 and the output signal Y = 1.
At t4, Y = 0 because the input signal Cnt = 0 even though the counter is still in state Q1Q0 = 11.



THANK YOU