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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB302–VLSI DESIGN

III YEAR/ V SEMESTER

UNIT 2 –COMBINATIONAL LOGIC CIRCUITS

TOPIC 9 –Design for low power principles

OUTLINE

- Power and Energy
- Dynamic Power Reduction
- Activity
- Static Power
- Low Power Design Principles
- Assessment
- Summary

Power and Energy

- Power is drawn from a voltage source attached to the V_{DD} pin(s) of a chip.

- Instantaneous Power: $P(t) = i_{DD}(t)V_{DD}$

- Energy: $E = \int_0^T P(t)dt = \int_0^T i_{DD}(t)V_{DD}dt$

- Average Power: $P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}dt$

Dynamic Power Reduction

- Dynamic Power Reduction (P_d)

Y

$$P_d = \alpha C V_{DD}^2 f_{clk}$$

$f\ clk$ ---.> *Clock Frequency*

α ---.> *Activity factor*

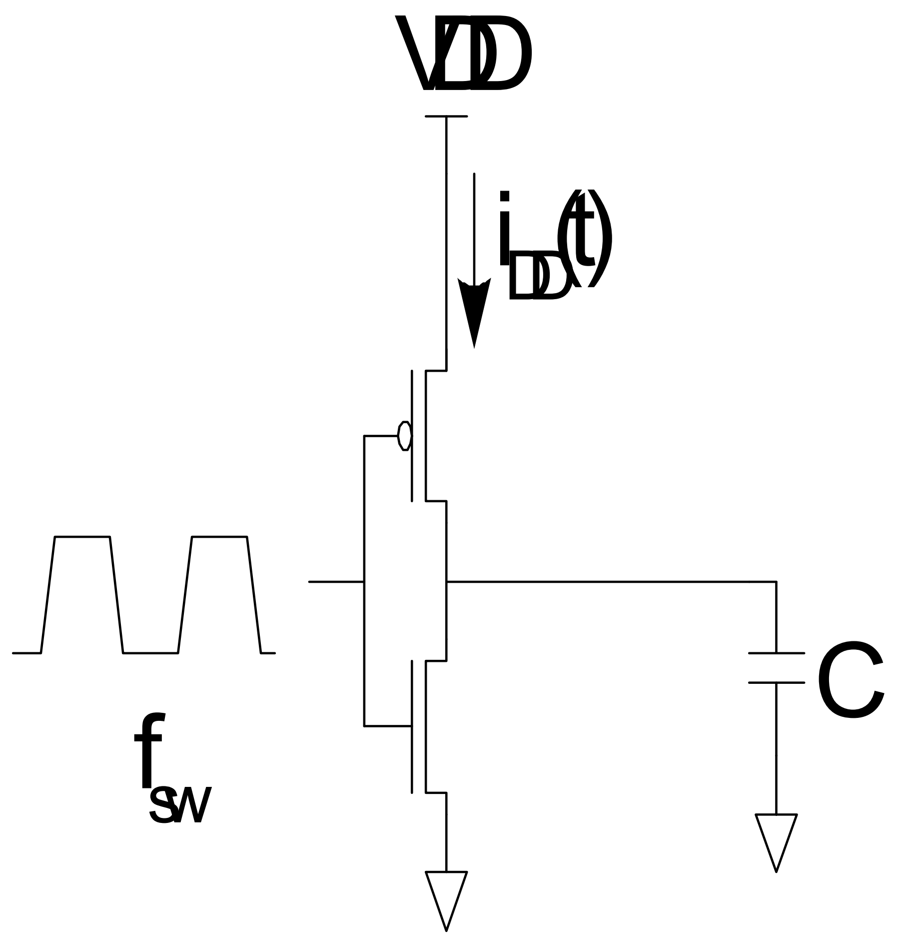
C ---.> *Switching Capacitance*

Dynamic Power Reduction

- If the chip is active, dynamic power dissipation is high.
- Pd is reduced by reducing α ,C V_{DD} or fclk.
- Clock gating is used to stop portions of the IC that are idle.
- Device switching capacitance can be reduced by using small transistors.
- Internet switching capacitance can be reduced by proper floor planning.
- If low power supply is used, then the power consumption is reduced
- When more transistors are operated in a velocity saturated region. So, the performance will not be reduced due to low power supply.

Dynamic Power

- Dynamic power is required to charge and discharge load capacitances when transistors switch.
- One cycle involves a rising and falling output.
- On rising output, charge $Q = CV_{DD}$ is required
- On falling output, charge is dumped to GND
- This repeats Tf_{sw} times over an interval of T



Dynamic Power Cont.

$$P_{dynamic} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}\,dt$$

$$= \frac{V_{DD}}{T}\int_0^T i_{DD}(t)\,dt$$

$$= \frac{V_{DD}}{T}\left[T f_{sw} C V_{DD}\right]$$

$$= C V_{DD}{}^2 f_{sw}$$

Activity Factor

Suppose the system clock frequency = f

Let $f_{sw} = \alpha f$, where α = activity factor

- If the signal is a clock, $\alpha = 1$
- If the signal switches once per cycle, $\alpha = ½$
- Dynamic gates:
  - Switch either 0 or 2 times per cycle, $\alpha = ½$
- Static gates:
  - Depends on design, but typically $\alpha = 0.1$

Short Circuit Current

- When transistors switch, both nMOS and pMOS networks may be momentarily ON at once
- Leads to a blip of “short circuit” current.
- < 10% of dynamic power if rise/fall times are comparable for input and output

Example

- 200 Mtransistor chip
  - 20M logic transistors
    - Average width: 12 λ
  - 180M memory transistors
    - Average width: 4 λ
- 1.2 V 100 nm process
  - C_g = 2 fF/μm

Dynamic Example

- Static CMOS logic gates: activity factor = 0.1

Memory arrays: activity factor = 0.05 (many banks!)

- Estimate dynamic power consumption per MHz.

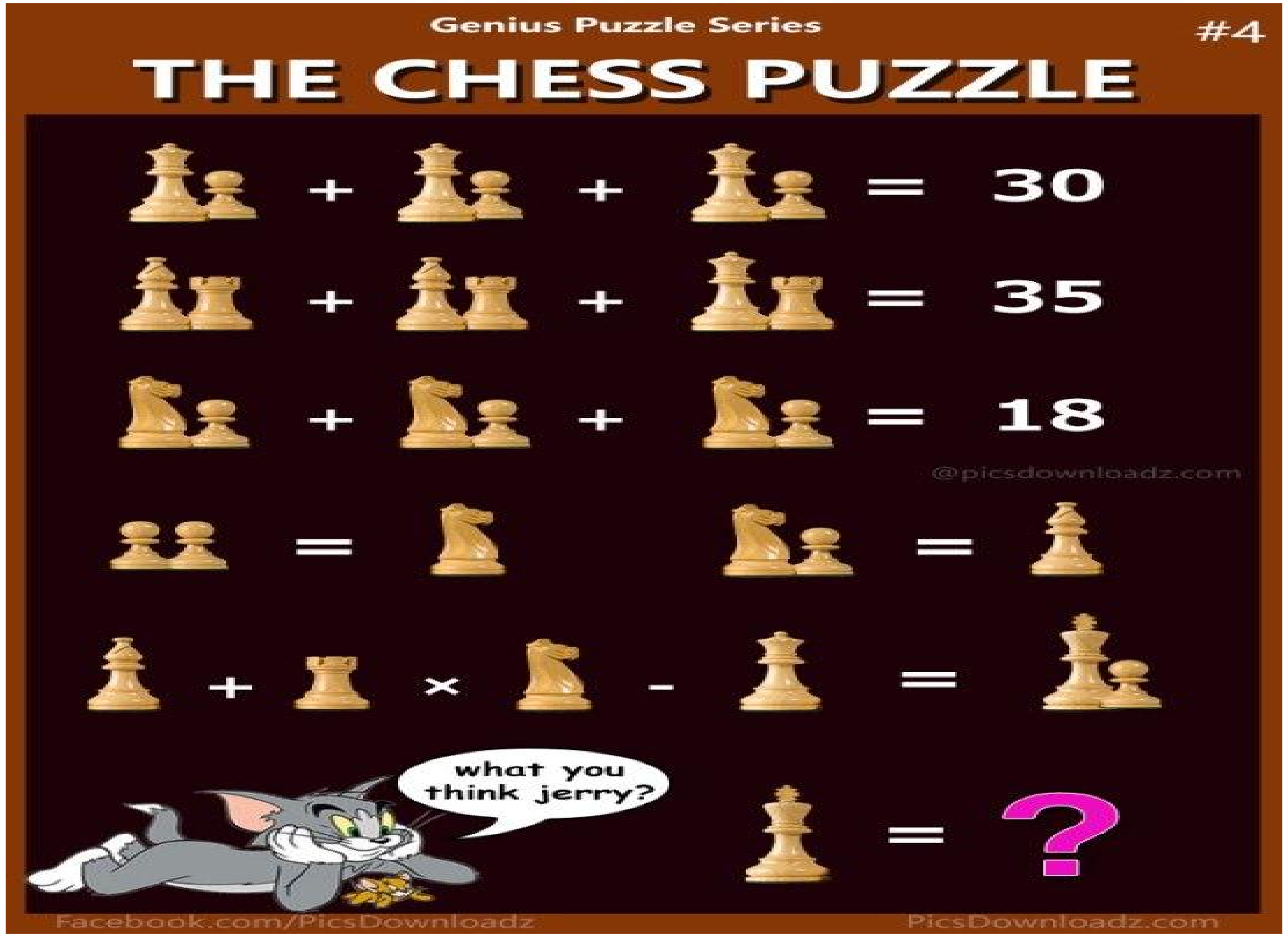
Neglect wire capacitance.

$$C_{\text{logic}} = \left(20 \times 10^6\right)(12\lambda)(0.05\mu m/\lambda)(2\,fF/\mu m) = 24nF$$

$$C_{\text{mem}} = \left(180 \times 10^6\right)(4\lambda)(0.05\mu m/\lambda)(2\,fF/\mu m) = 72nF$$

$$P_{\text{dynamic}} = \left[0.1C_{\text{logic}} + 0.05C_{\text{mem}}\right](1.2)^2 f = 8.6 \text{ mW/MHz}$$

Activity



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Static Power

- More static power is consumed by pseudo – n MOS gates.
- Static power is consumed even when chip is quiescent.

 - Ratioed circuits burn power in fight between ON

-TransistorsLeakage draws power from nominally OFF devices.

- Three parameters

    1. Supply Voltage
    2. Level Converter
    3. Capacitance

Ratio Example

The chip contains a 32 word x 48 bit ROM

Uses pseudo-nMOS decoder and bitline pullups

one wordline and 24 bitlines are high

Find static power drawn by the ROM

$\beta = 75\ \mu A/V^2$

$V_{tp} = -0.4V$

Solution

$$I_{\text{pull-up}} = \beta \frac{\left(V_{DD} - \left|V_{tp}\right|\right)^2}{2} = 24\mu\text{A}$$

$$P_{\text{pull-up}} = V_{DD} I_{\text{pull-up}} = 29\mu\text{W}$$

$$P_{\text{static}} = (31 + 24) P_{\text{pull-up}} = 1.6\ \text{mW}$$

Leakage Example

- The process has two threshold voltages and two oxide thicknesses.
- Subthreshold leakage:
  - 20 nA/μm for low V_t
  - 0.02 nA/μm for high V_t
- Gate leakage:
  - 3 nA/μm for thin oxide
  - 0.002 nA/μm for thick oxide
- Memories use low-leakage transistors everywhere
- Gates use low-leakage transistors on 80% of logic

Leakage Example

- Estimate static power:
  - High leakage: $\left(20\times10^{6}\right)(0.2)(12\lambda)(0.05\mu m/\lambda)=2.4\times10^{6}\mu m$
  - Low leakage: $\left(20\times10^{6}\right)(0.8)(12\lambda)(0.05\mu m/\lambda)+\left(180\times10^{6}\right)(4\lambda)(0.05\mu m/\lambda)=45.6\times10^{6}\mu m$

$$
\begin{aligned}
I_{static} &= \left(2.4\times10^{6}\mu m\right)\left[(20nA/\mu m)/2+(3nA/\mu m)\right]+ \\
&\quad \left(45.6\times10^{6}\mu m\right)\left[(0.02nA/\mu m)/2+(0.002nA/\mu m)\right] \\
&= 32mA \\
P_{static} &= I_{static}V_{DD} = 38mW
\end{aligned}
$$

- if no low leakage devices, P_{static} = 749 mW (!)

Low Power Design principles

Reduce dynamic power

α: clock gating, sleep mode

C: small transistors (esp. on clock), short wires

V_{DD}: lowest suitable voltage

f: lowest suitable frequency

Reduce static power

Selectively use ratioed circuits

Selectively use low V_t devices

Leakage reduction:

stacked devices, body bias, low temperature

Assessment

- **Reduce dynamic power---????????**
  - α:
  - C:
  - V_{DD}:
  - F:
- **Reduce static power-Fill up the blanks???**
  - Selectively use ---------------circuits
  - Selectively use low -------devices
  - -------- reduction:

    -------devices, ------ bias,------ temperature

THANK YOU