SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

COIMBATORE-35

DEPARTMENT OF COMPUTER SCIENE AND ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Multiple Choice Questions with Answers

1. What would be the minterm expansion of the following:

f(P, Q, R) = PQ + QR' + PR'

a. m0 + m1 + m3 + m5

b. m2 + m4 + m6 + m7

c. m2 + m3 + m4 + m5

d. m0 + m1 + m6 + m7

Answer: (b) m2 + m4 + m6 + m7

2. What is the hexadecimal representation of 6578?

a. D71

b. 32F

c. 1AF

d. D78

Answer: (c) 1AF

3. Let us consider an array multiplier used for the multiplication of two n bit numbers. In case every gate in the circuit faces a unit delay, then the total delay of this multiplier would be:

a. Θ(n)

b. Θ(1)

c. Θ(n^2)

d. Θ(log n)

Answer: (a) Θ(n)

4. What would be the total prime implicants of the following function:

f(w, x, y, z) = Σ(0, 2, 4, 5, 6, 10)

a. 5

b. 4

c. 3

d. 2

Answer: (c) 3

5. How many pulses do we need if we want to change the contents of any given 8-bit up counter from the bit 10101100 to bit 00100111 (the rightmost bit here is the LSB)?

a. 123

b. 124

c. 133

d. 134

Answer: (a) 123

6. When we add a two's complement, 4-bit, binary numbers 1101 and 0100, it would result in:

a. 1001 and no overflow

b. 0001 and an overflow

c. 1001 and an overflow

d. 0001 and no overflow

Answer: (d) 0001 and no overflow

7. If we want to put an 8085 microprocessor in a wait state, then we have:

a. to raise the-HOLD input

b. to raise the READY input

c. to lower the HOLD input

d. to lower the READY input

Answer: (d) to lower the READY input

8. What would be the 2's complement representation (in hexadecimal) of (−539)10?

a. 9E7

b. DE5

c. DBC

d. ABE

Answer: (b) DE5

9. What would be the 2′ s complement representation of the -15 decimal value?

a. 10001

b. 1111111

c. 1001

d. 1111

Answer: (d) 1111

10. If in a base-x type of number system, 73x is equivalent to that of 54y in a base-y type of number system, then the possible values of both- x and y would be:

a. 10, 12

b. 8, 16

c. 8, 11

d. 9, 13

Answer: (c) 8, 11

11. In the Principle of locality, there is a justification of the use of:

a. DMA

b. Cache memory

c. Threads

d. Interrupts

Answer: (b) Cache memory

12. Which of these is NOT involved in the case of a memory write operation?

a. Databus

b. MDR

c. MAR

d. PC

Answer: (d) PC

13. Which of these is required when we want to establish the communication links between a CPU and its peripherals?

a. Memory data register

b. Memory address register

c. Instruction register

d. Index register

Answer: (a) Memory data register

14. A given 2 level memory consists of a 30 ns average access time. If the cache, as well as the memory access time here, is 20 ns and 150 ns, respectively, what would be the hit ratio?

a. 99%

b. 70%

c. 93%

d. 80%

Answer: (c) 93%

15. If we double the cache line length and it reduces the miss rate to 3%, then by how much will the average memory access time be reduced?

a. 4.85 ns

b. 22.2 ns

c. 25.75 ns

d. 27.1 ns

Answer: (d) 27.1 ns

16. The total number of digits that are required for the representation of a 126-bit binary number in its decimal form would be:

a. 46 bits

b. 42 bits

c. 36 bits

d. 32 bits

Answer: (b) 42 bits

17. Which of these memories would have the lowest access time in a system:

a. Main Memory

b. Magnetic Disk

c. Registers

d. Cache

Answer: (c) Registers

18. Which of these refers to the minimization expression for the following:

A+A’B+A’B’C+A’B’C’D

a. A+B) (C+D)

b. ABCD

c. 1

d. A+B+C+D

Answer: (d) A+B+C+D

19. What is the minimum time delay present between the initiations of two separate, independent memory operations known as?

a. Cycle Time

b. Latency Time

c. Access Time

d. Transfer Rate

Answer: (a) Cycle time

20. Which of these addressing modes is the most suitable for some high-level language statements?

a. Indexed

b. Auto-decrement

c. Auto-increment

d. Displacement

Answer: (b) Auto-decrement

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