



# **SNS COLLEGE OF TECHNOLOGY**

**Coimbatore-35**  
**An Autonomous Institution**



Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade  
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

## **DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING**

### **19ECB231 DIGITAL ELECTRONICS**

II YEAR/ III SEMESTER

### **UNIT-IV DESIGN OF SEQUENTIAL CIRCUITS**

**Topic 1- Registers , Shift Registers, Universal Shift Registers**



## IDENTIFY THE TOPIC

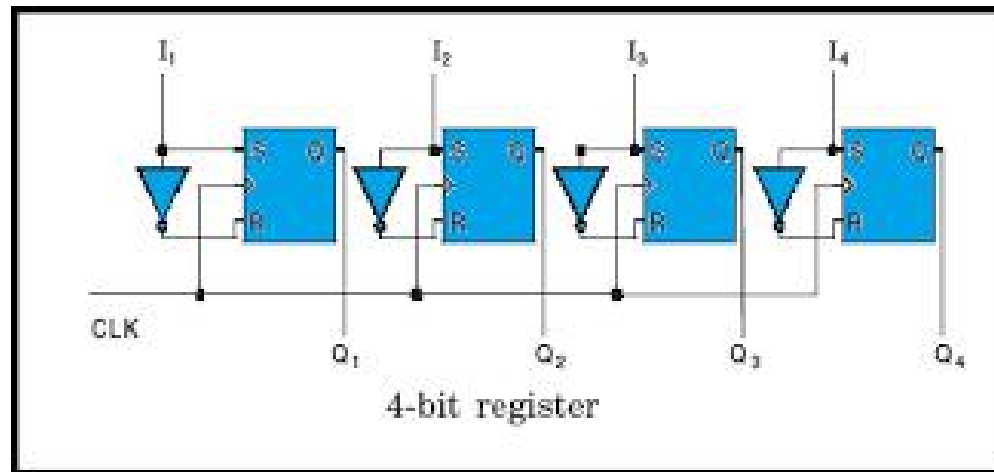




## Registers



- Flip flops can be used to store a single bit of binary data (1 or 0).
- However, in order to store multiple bits of data, we need multiple flip flops.
- N flip flops are to be connected in an order to store n bits of data.
- A Register is a device which is used to store such information.
- It is a group of flip flops connected in series used to store multiple bits of data.





## Types of Registers

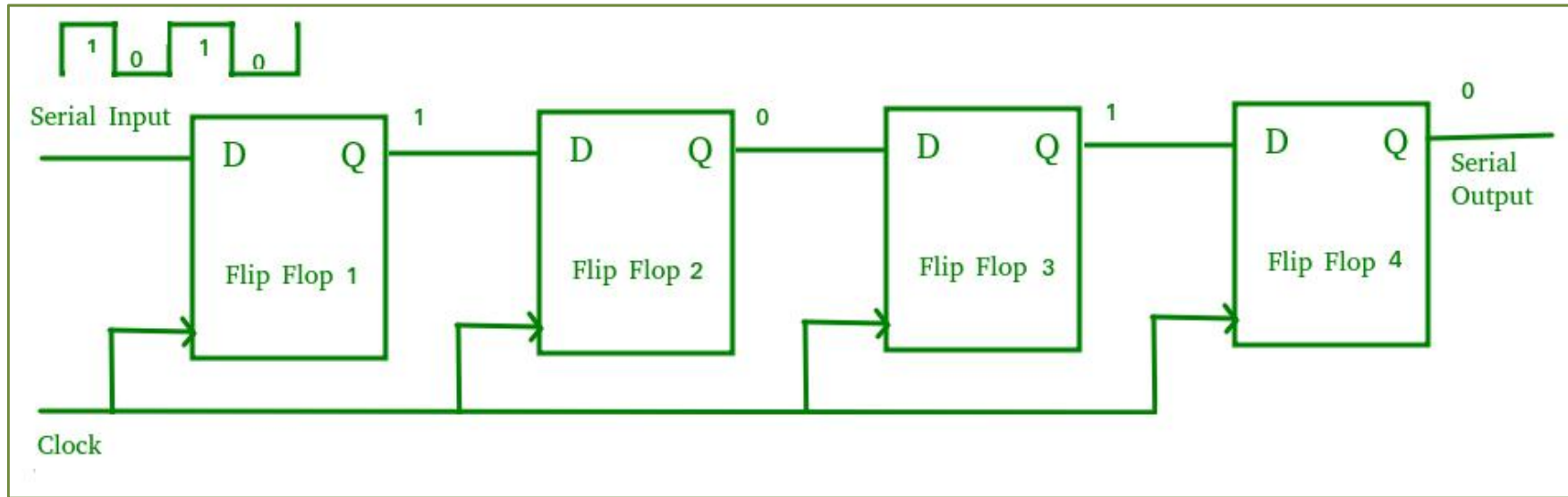


Shift registers are basically of 4 types. These are:

- Serial In Serial Out shift register
- Serial In parallel Out shift register
- Parallel In Serial Out shift register
- Parallel In parallel Out shift register



# Serial In Serial Out shift register





## Serial In Serial Out shift register

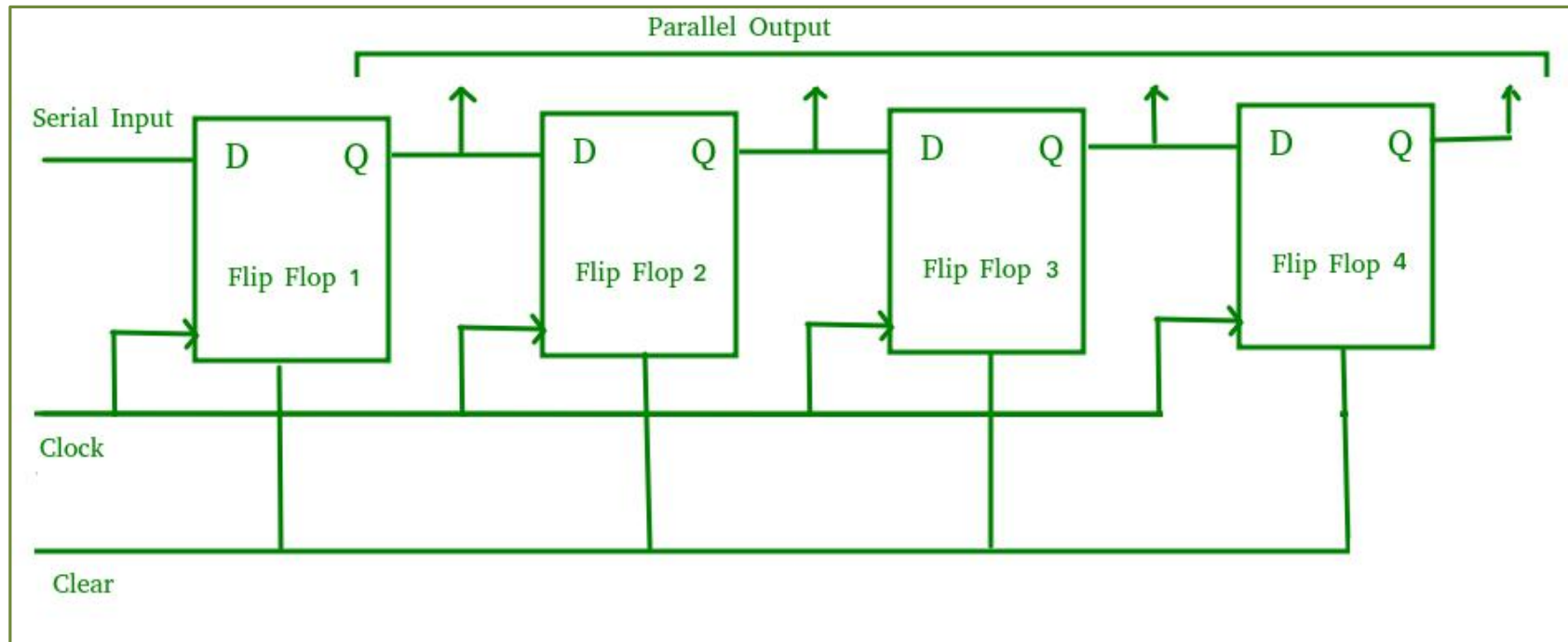


Operation of the Shift-right Register

Timing pulse	$Q_A$	$Q_B$	$Q_C$	$Q_D$	Serial output at $Q_D$
Initial value	0	0	0	0	0
After 1 <sup>st</sup> clock pulse	1	0	0	0	0
After 2 <sup>nd</sup> clock pulse	1	1	0	0	0
After 3 <sup>rd</sup> clock pulse	0	1	1	0	0
After 4 <sup>th</sup> clock pulse	1	0	1	1	1



# Serial-In Parallel-Out shift Register (SIPO)





# Serial-In Parallel-Out shift Register (SIPO)

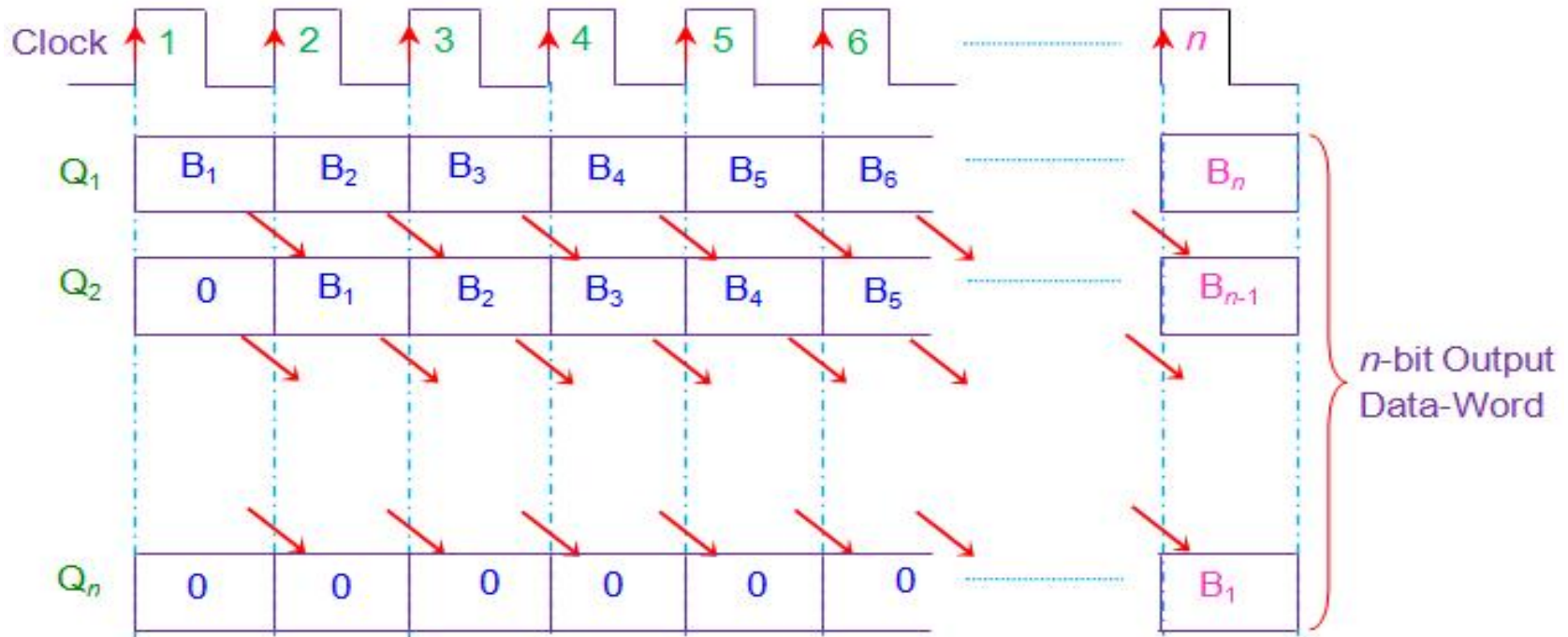
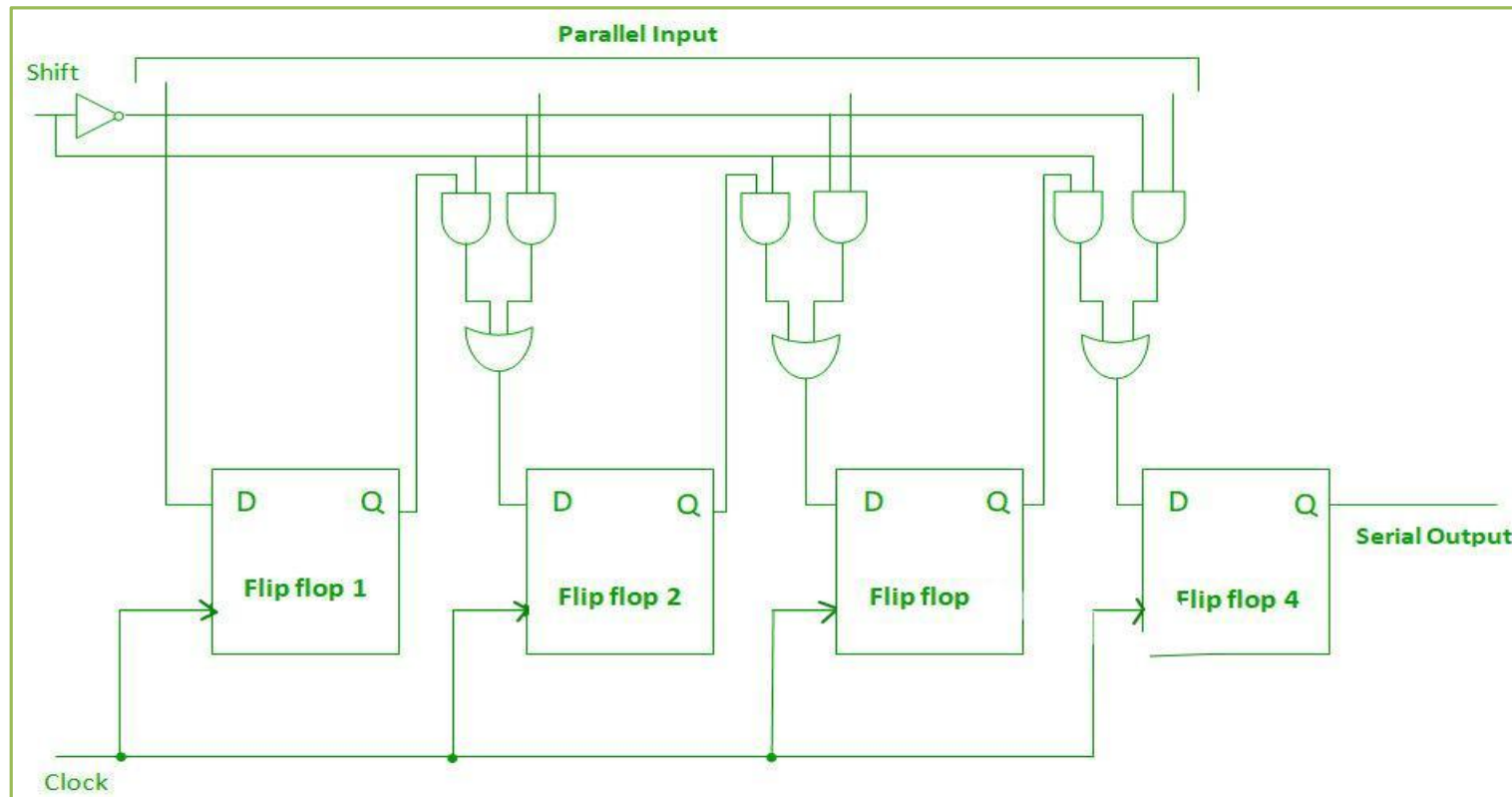


Figure 2 Output Waveform of  $n$ -bit Right-Shift SIPO Shift Register





# Parallel-In Serial-Out Shift Register (PISO)





## Parallel-In Serial-Out Shift Register (PISO)



Table I Data Movement in Right-Shift PISO Shift

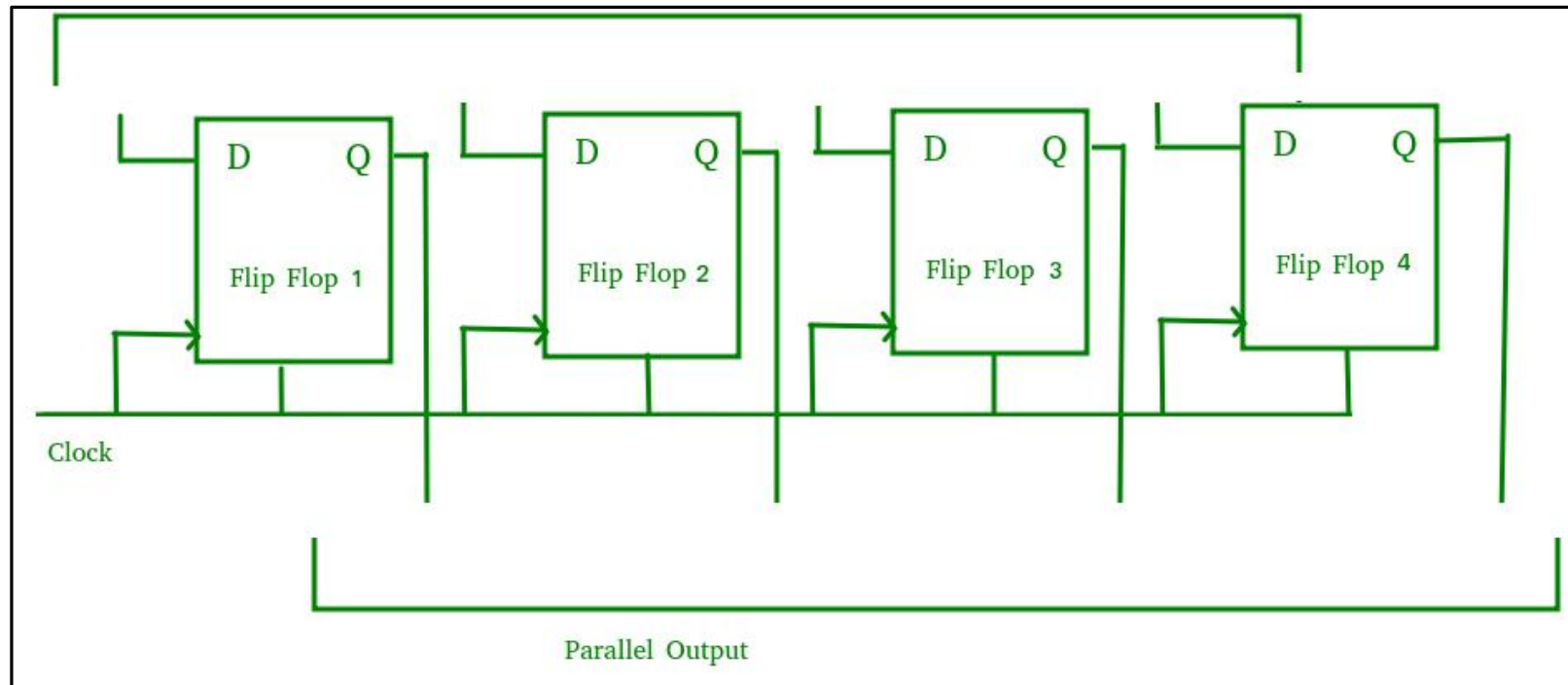
Clock Cycle	SH / $\overline{LD}$	$Q_1$	$Q_2$	$Q_3$	...	$Q_{n-1}$	$Q_n =$ Data out
1	0	$B_1$	$B_2$	$B_3$	...	$B_{n-1}$	$B_n$
2	1	0	$B_1$	$B_2$	...	$B_{n-2}$	$B_{n-1}$
3	1	0	0	$B_1$	...	$B_{n-3}$	$B_{n-2}$
⋮		⋮	⋮	⋮	...	⋮	⋮
⋮		⋮	⋮	⋮	...	⋮	⋮
⋮		⋮	⋮	⋮	...	⋮	⋮
$n-1$	1	0	0	0	...	$B_1$	$B_2$
$n$	1	0	0	0	...	0	$B_1$

Parallel data Loading Operation

Serial data retrieval



## Parallel-In Parallel-Out Shift Register (PIPO)





# Parallel-In Parallel-Out Shift Register (PIPO)



Table I Data Movement in Right-Shift PIPO Shift Register

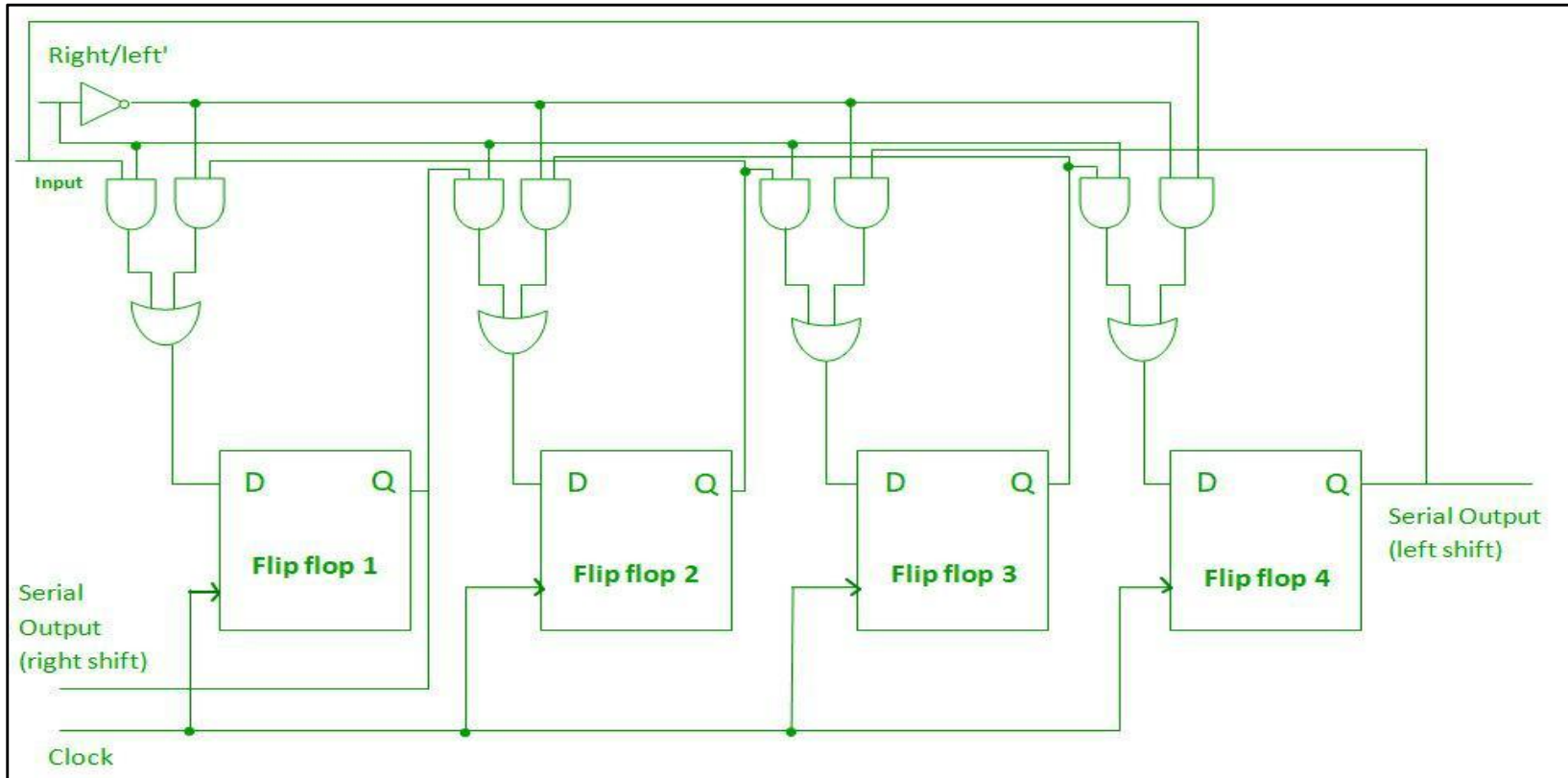
Clock Cycle	SH / $\overline{\text{LD}}$	$Q_1$	$Q_2$	$Q_3$	...	$Q_{n-1}$	$Q_n$
1	0	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>		B <sub>n-1</sub>	B <sub>n</sub>
2	1	0	B <sub>1</sub>	B <sub>2</sub>	...	B <sub>n-2</sub>	B <sub>n-1</sub>
3	1	0	0	B <sub>1</sub>	...	B <sub>n-3</sub>	B <sub>n-2</sub>
⋮		⋮	⋮	⋮	...	⋮	⋮
⋮		⋮	⋮	⋮	...	⋮	⋮
⋮		⋮	⋮	⋮	...	⋮	⋮

Parallel Data Loading

Parallel Data Retrieval



# Bidirectional Shift Register





# Bidirectional Shift Register

Clock Cycle	CLR	R / $\bar{L}$	$Q_1$	$Q_2$	...	$Q_{n-1}$	$Q_n$
1	0	1	B <sub>1</sub>	0		0	0
2	0	1	B <sub>2</sub>	B <sub>1</sub>		0	0
⋮	⋮	⋮	⋮	⋮		⋮	⋮
⋮	⋮	⋮	⋮	⋮	...	⋮	⋮
⋮	⋮	⋮	⋮	⋮		⋮	⋮
n	0	1	B <sub>n</sub>	B <sub>n-1</sub>	...	B <sub>2</sub>	B <sub>1</sub>
n+1	1	X	0	0	...	0	0
n+2	0	0	0	0	...	0	B <sub>1</sub>
n+3	0	0	0	0	...	B <sub>1</sub>	B <sub>2</sub>
n+4	0	0	0	0	...	B <sub>2</sub>	B <sub>3</sub>
⋮	⋮	⋮	⋮	⋮	...	⋮	⋮
⋮	⋮	⋮	⋮	⋮	...	⋮	⋮
⋮	⋮	⋮	⋮	⋮	...	⋮	⋮

} Right-Shift of Data Bits

} Register is Cleared

} Left-Shift of Data Bits

**Table I** Data Movement in Bidirectional Shift Register

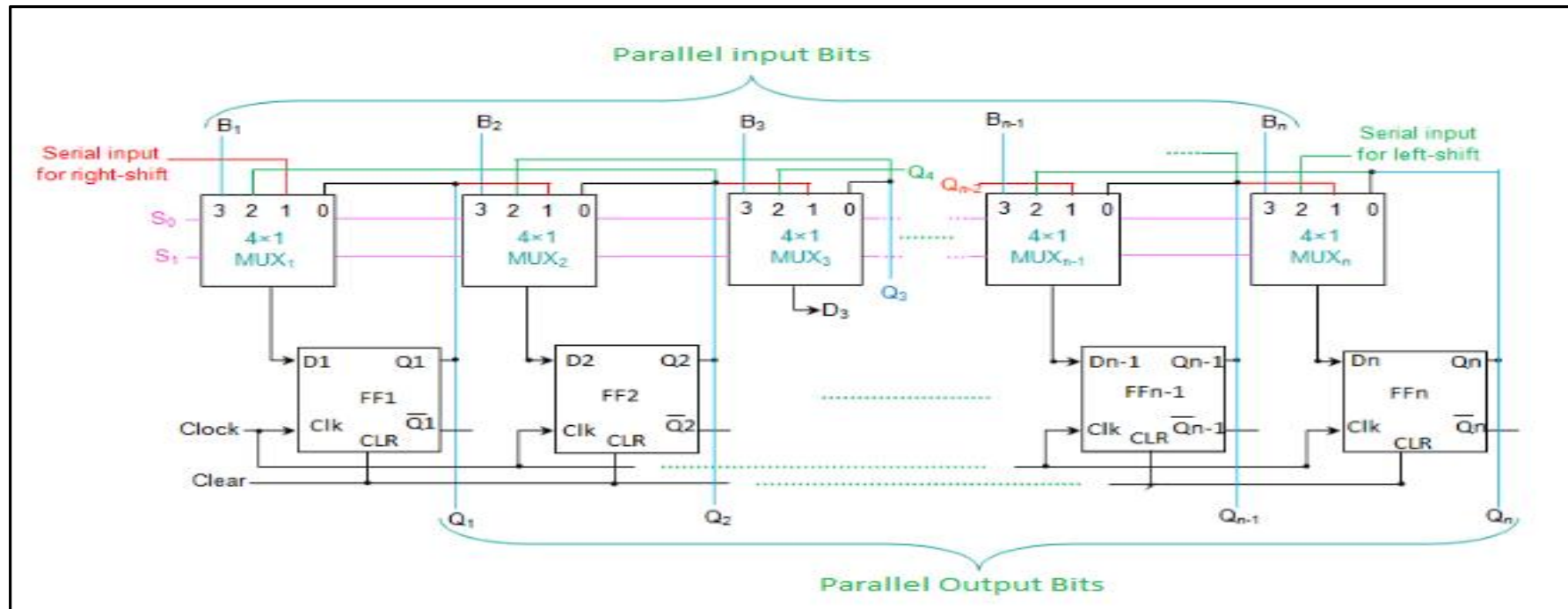




# Universal Shift Register



A Universal shift register is a register which has both the right shift and left shift with parallel load capabilities. Universal shift registers are used as memory elements in computers. A Unidirectional shift register is capable of shifting in only one direction.





# Universal Shift Register



Table II Truth Table for  $n$ -bit Universal Shift Register

Serial Input for Left Shift			$L_1L_2...L_n$					
Serial Input for Right Shift			$R_1R_2...R_n$					
Parallel Input			$B_1B_2...B_n$					
Clk	CLR	Mux Output	Outputs					
			$Q_1$	$Q_2$	---	$Q_{n-1}$	$Q_n$	
1	1	X	0	0	---	0	0	Register is Cleared
2	0	1	$R_1$	0	---	0	0	
3	0	1	$R_2$	$R_1$	---	0	0	Right-shift of Data Bits
...	...	...	...	...	---	...	...	
...	...	...	...	...	---	...	...	
$n+1$	0	1	$R_n$	$R_{n-1}$	---	$R_2$	$R_1$	
$n+2$	1	X	0	0	---	0	0	Register is Cleared
$n+3$	0	2	0	0	---	0	$L_1$	
$n+4$	0	2	0	0	---	$L_1$	$L_2$	Left-shift of Data Bits
...	...	...	...	...	---	...	...	
...	...	...	...	...	---	...	...	
$2n+2$	0	2	$L_1$	$L_2$	---	$L_{n-1}$	$L_n$	
$2n+3$	0	0	$L_1$	$L_2$	---	$L_{n-1}$	$L_n$	No Change
$2n+4$	0	0	$L_1$	$L_2$	---	$L_{n-1}$	$L_n$	
$2n+5$	0	3	$B_1$	$B_2$	---	$B_{n-1}$	$B_n$	
...	...	...	...	...	---	...	...	





## Application of Shift Register



- The shift registers are used for temporary data storage.
- The shift registers are also used for data transfer and data manipulation.
- The serial-in serial-out and parallel-in parallel-out shift registers are used to produce time delay to digital circuits.
- The serial-in parallel-out shift register is used to convert serial data into parallel data thus they are used in communication lines where demultiplexing of a data line into several parallel line is required.
- A Parallel in Serial out shift register is used to convert parallel data to serial data.



**THANK YOU**