Reg.No: | | | | | | | |

SNS College of Technology, Coimbatore-35.
(Autonomous)
B.E/B.Tech Internal Assessment -I
Academic Year 2023-2024(Odd)
Common to CSE, IT & AIML
Third Semester
19ECB231 – DIGITAL ELECTRONICS

B

Time: $1^{1/2}$ Hours **Maximum Marks: 50**

Answer All Questions

PART - A (5 x 2 = 10 Marks)

		CO	Blooms
1.	Convert Octal to binary: $(634)_8$	CO1	App
2.	Define principle of duality.	CO1	Rem
3.	What is meant by Minterm and Maxterm?	CO1	Rem
4.	List and define the Laws of Boolean Algebra.	CO2	Ana
5.	Analyze the Boolean expression for a half adder.	CO2	Ana

PART – B (2 x 13 = 26 Marks) (1 x 14 = 14 Marks)

				CO	Blooms
6.	(a)	(i) Simplify Y(A,B,C,D) = $\sum_m$ (0,1,2,4,8,10) + d(5,7) using Karnaugh Map. (ii) Construct the boolean expression using logic gates: **Y = B`C`+A`C`+AB**	8 5	CO1	Ana
		(or)			
	(b)	(i) Simplify the following expression using K-map F(A, B, C) = $\sum_m$(1,2,3,6,7) (ii) Simplify the boolean function: **(A+B)(A+B')(A'+C)**	8 5	CO1	Ana
7.	(a)	What is meant by Karnaugh map? Explain how karnaugh maps are constructed for (i) Two variables (ii) Three variables (iii) Four variables	13	CO1	Und
		(or)			

	(b)	Illustrate Half Subtractor and Full Subtractor with its Truth Table and Logical Diagram.	13	CO2	Und
8.	(a)	Examine the minimal Sum of Products for boolean function $F(a,b,c,d)=\sum_m(1,3,4,5,6,8,9,10,11)$ using Tabulation method	14	CO1	Ana
		(or)			
	(b)	(i) Develop a full adder using two half adders and an OR gate. (ii) Outline 4-bit Parallel binary subtractor.	7 7	CO2	App Und
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Abbreviations:

CO – Course Outcomes; **Rem-** Remembering; **Und –** Understanding; **App –** Applying; **Ana –** Analyzing.