Reg.No: | | | | | | | |

SNS College of Technology, Coimbatore-35.
(Autonomous)
B.E/B.Tech Internal Assessment -I
Academic Year 2023-2024(Odd)
Common to CSE, IT & AIML
Third Semester
19ECB231 – DIGITAL ELECTRONICS

A

Time: $1^{1/2}$ Hours **Maximum Marks: 50**

Answer All Questions

PART - A (5 x 2 = 10 Marks)

		CO	Blooms
1.	List the different types of number systems.	CO1	Rem
2.	State Demorgan's theorem.	CO1	Und
3.	Which gates are called Universal gates? Why it is called so?	CO1	Rem
4.	Outline the block diagram of combinational circuit.	CO2	App
5.	Difference between full adder and half adder.	CO2	Ana

PART – B (2 x 13 = 26 Marks) (1 x 14 = 14 Marks)

				CO	Blooms
6.	(a)	Reduce the following four variable function to its minimum Sum of Products Form: Y=A`B`CD`+ABCD`+AB`CD`+AB`CD+AB`C`D`+ABC`D`+A`B`CD+A`B`C`D`	13	CO1	App
		(or)			
	(b)	(i) Reduce the following expression using K-map F(a, b, c) = $\sum_m(0, 2, 6, 7)$ (ii) Simplify the Boolean function : AB+A`C+BC = AB+A`C	7 6	CO1	Ana Rem
7.	(a)	(i) Explain logic gates with appropriate Logic diagram and Truth Table. (ii) State and Prove the laws of Boolean Algebra	7 6	CO1	Und
		(or)			

	(b)	(i) How will you design a full subtractor using two half subtractors and an OR gate. (ii) Outline 4-bit Parallel binary adder.	7 6	CO2	Ana
8.	(a)	Find the Minimal Sum of Product for the Boolean Expression $Y(A,B,C,D)=\sum_m(1,2,3,7,8,9,10,11,14,15)$ using Quine Mc-cluskey Method.	14	CO1	U
		(or)			
	(b)	Draw and explain Half Adder and Full Adder with necessary truth tables and logic gates.	14	CO2	Ana

Abbreviations:

CO – Course Outcomes; **Rem-** Remembering; **Und –** Understanding; **App –** Applying; **Ana –** Analyzing;