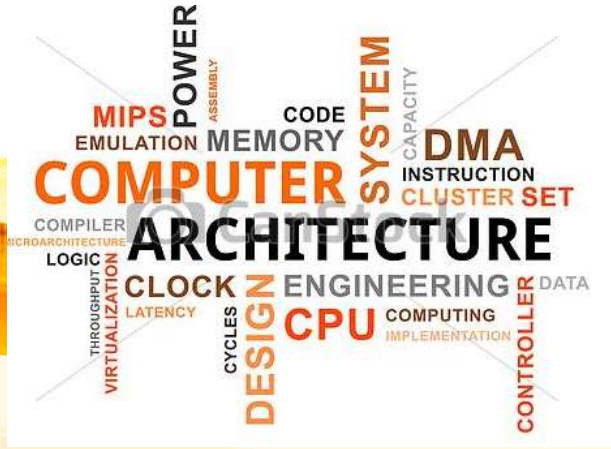
UNIT III
PROCESSOR AND PIPELINING

Fundamental concepts – Execution of a complete instruction – Multiple bus organization – Hardwired control – Micro programmed control – Pipelining: Basic concepts – Data hazards – Instruction hazards – Influence on Instruction sets – **Data path and control consideration.**

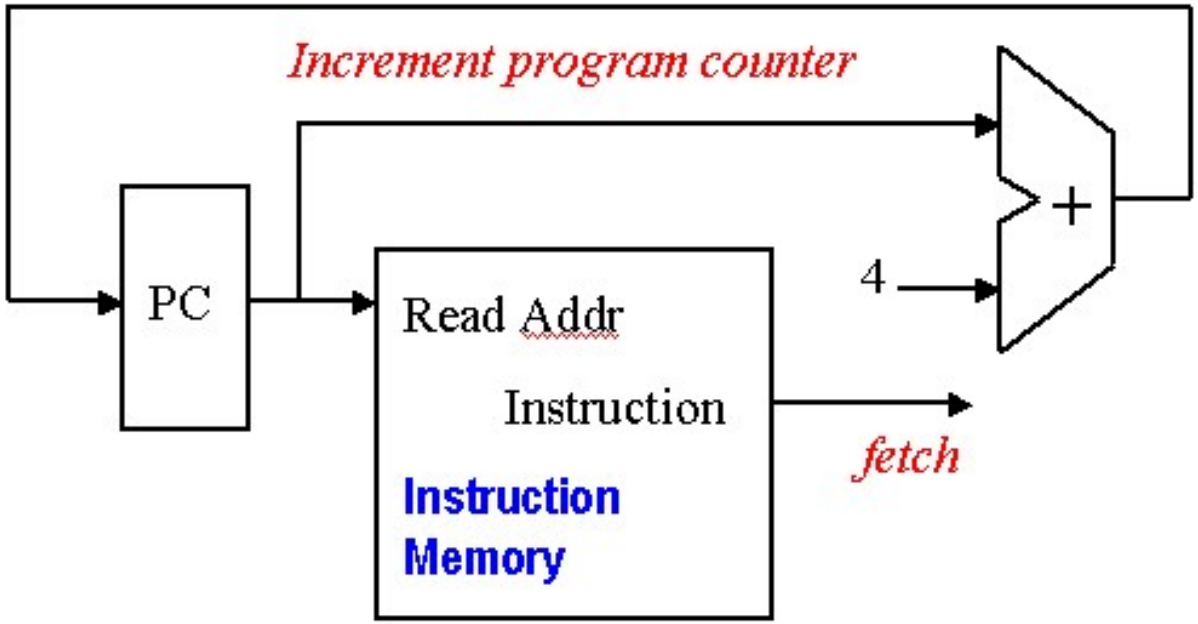


Recap the previous Class

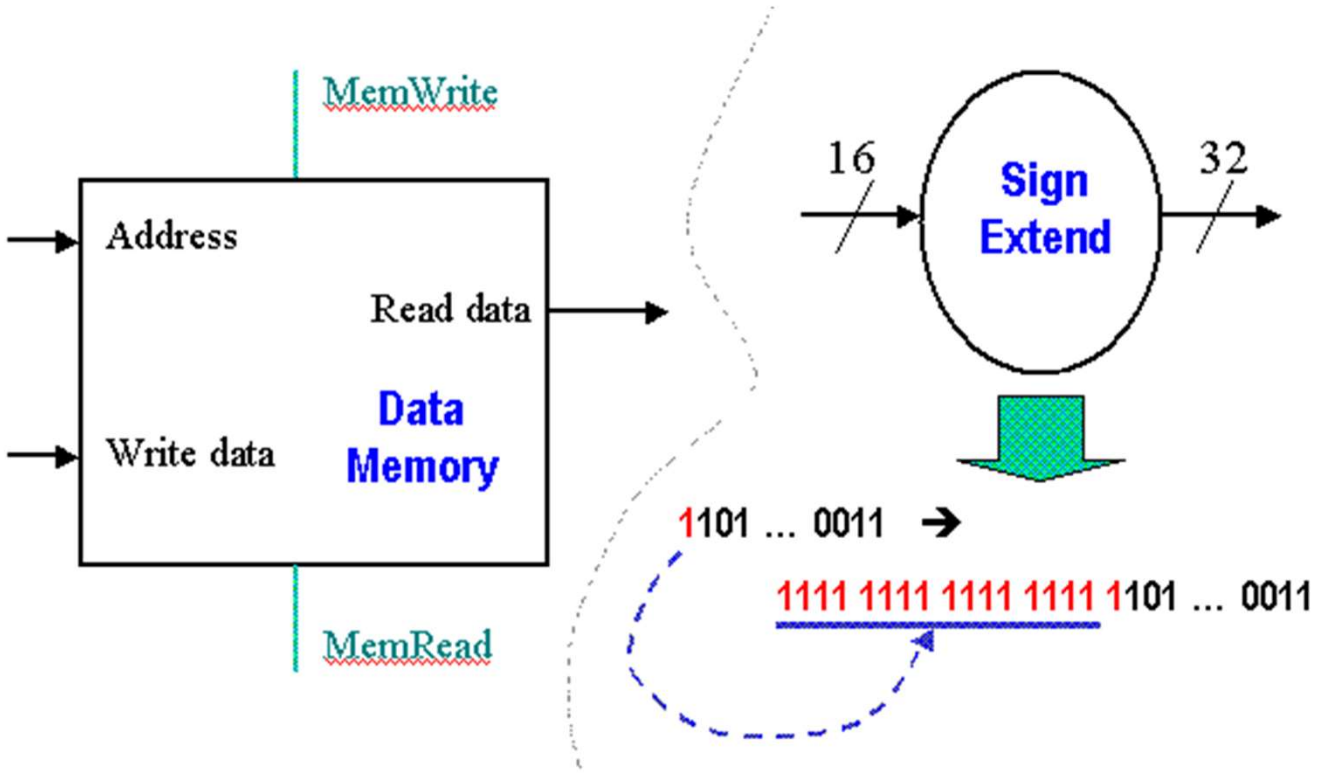
Data path and control

- ***Datapath*** is the hardware that performs all the required operations, for example, ALU, registers, and internal buses.
- ***Control*** is the hardware that tells the Datapath what to do, in terms of switching, operation selection, data movement between ALU components, etc.

Reading Assignment

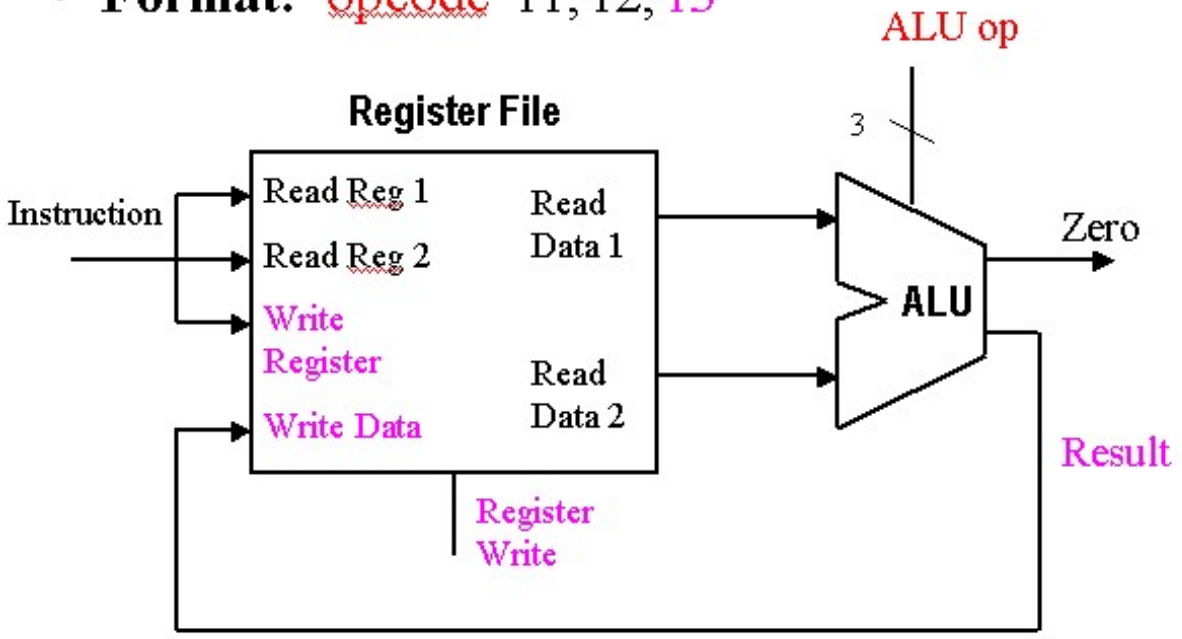


Data Memory and Sign Extender

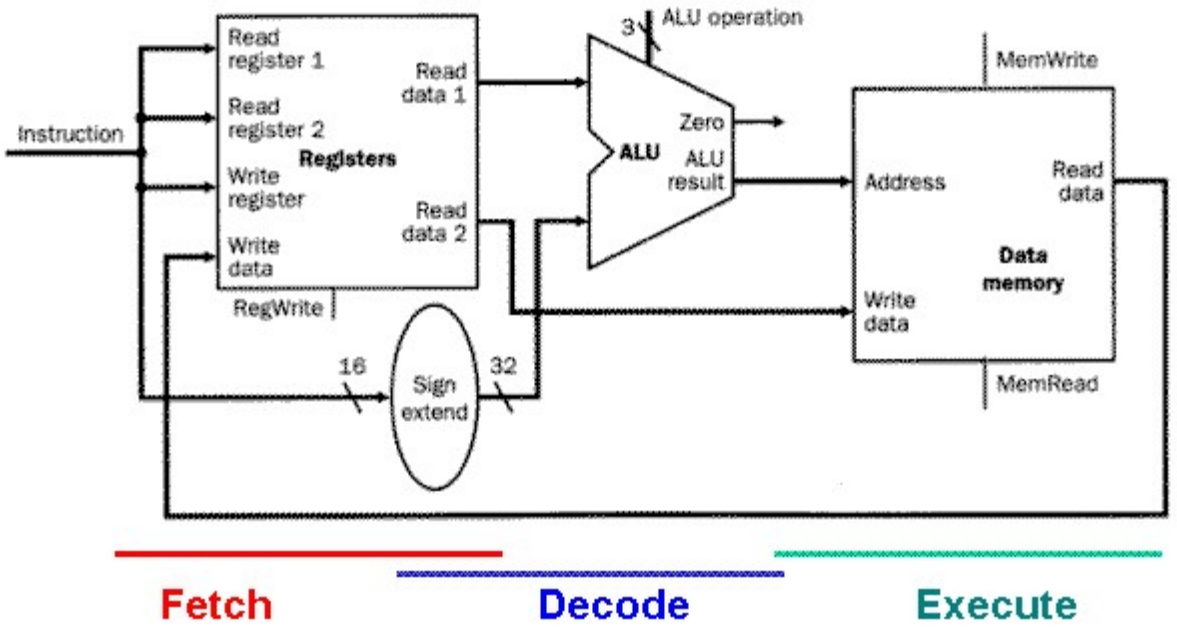


R-format Datapath

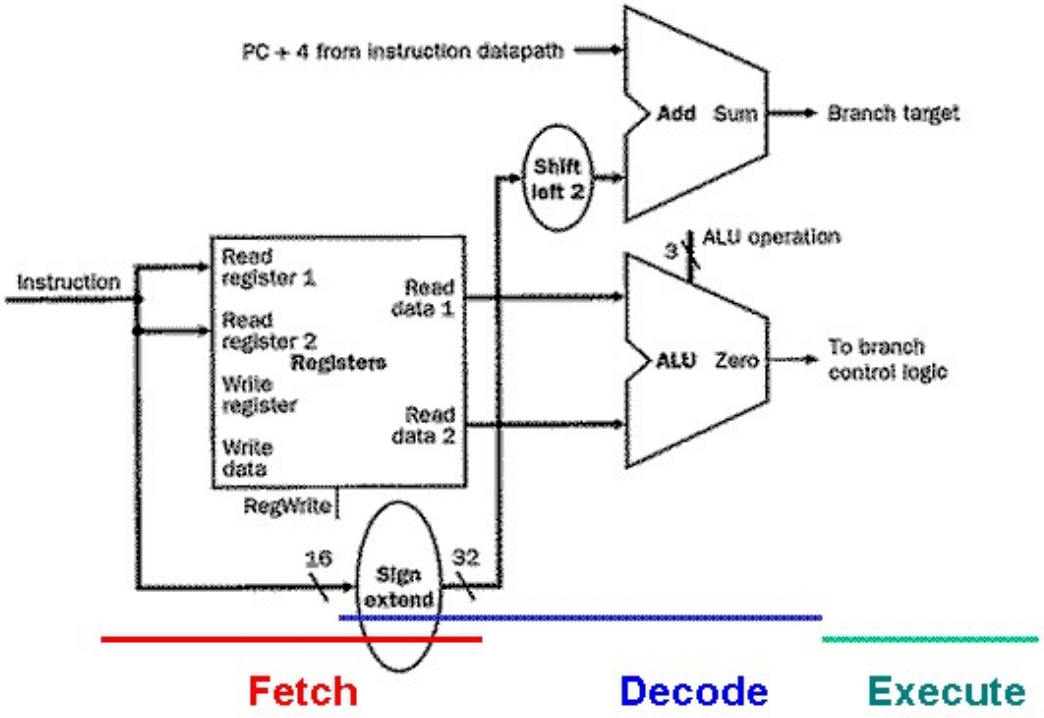
- **Format:** opcode r1, r2, r3



Load/Store Datapath



Branch/Jump Datapath

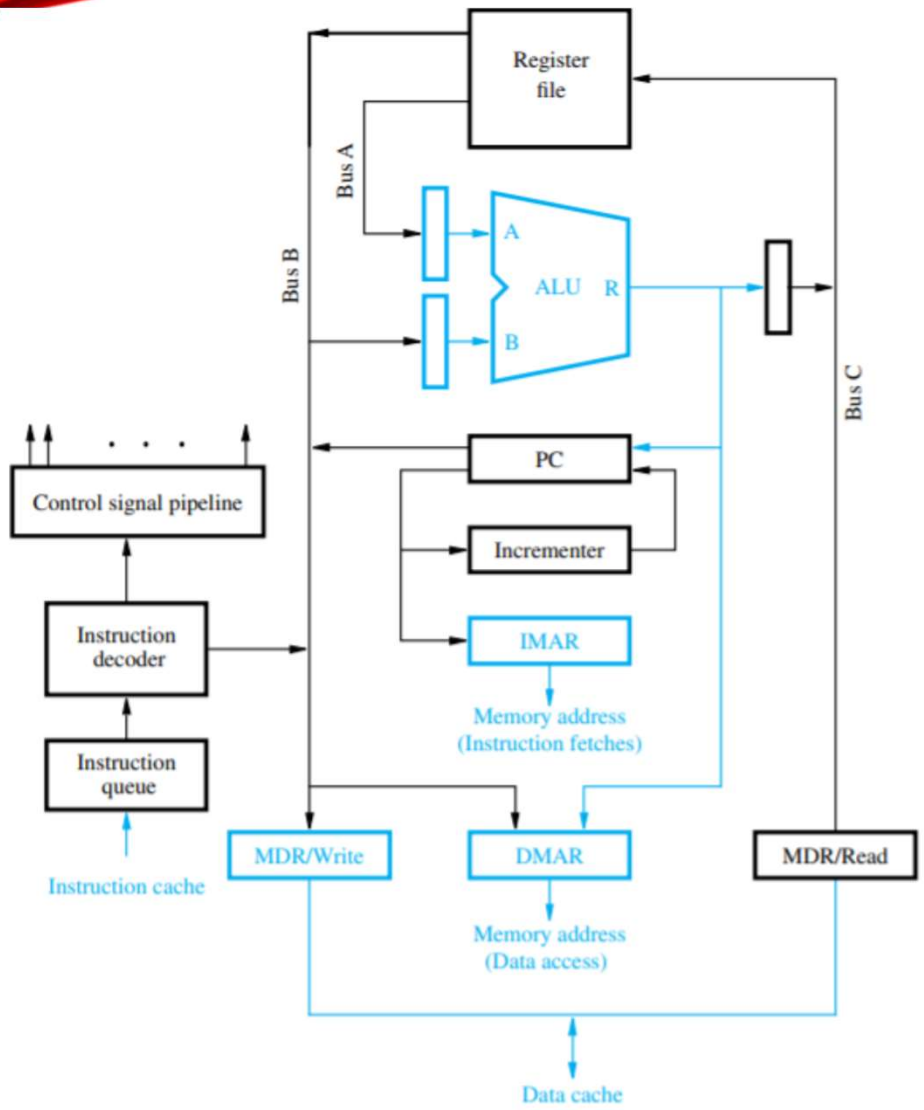


Datapath and Control Considerations

- Separate instruction and data caches
- PC is connected to IMAR
- DMAR
- Separate MDR
- Buffers for ALU
- Instruction queue
- Instruction decoder output

- Reading an instruction from the instruction cache
- Incrementing the PC
- Decoding an instruction
- Reading from or writing into the data cache
- Reading the contents of up to two registers from the register file
- Writing into one register in the register file
- Performing an ALU operation

Datapath and Control Considerations




Thank You