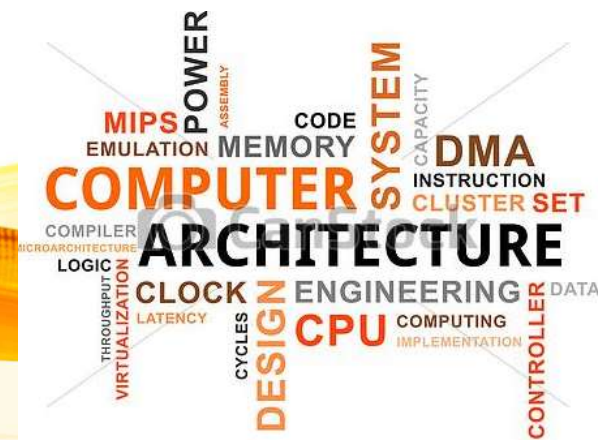


UNIT III

PROCESSOR AND PIPELINING

Fundamental concepts – Execution of a complete instruction – Multiple bus organization – **Hardwired control** – Micro programmed control – Pipelining: Basic concepts – Data hazards – Instruction hazards – Influence on Instruction sets – Data path and control consideration.



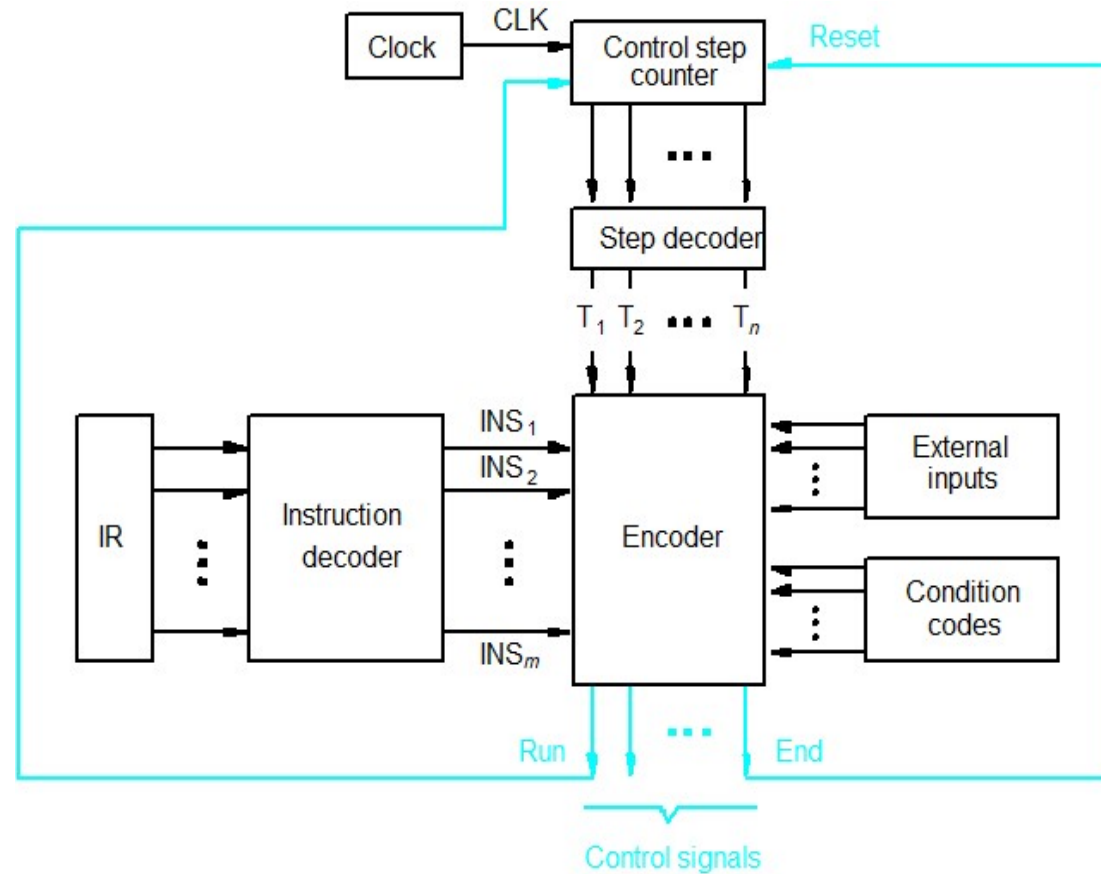
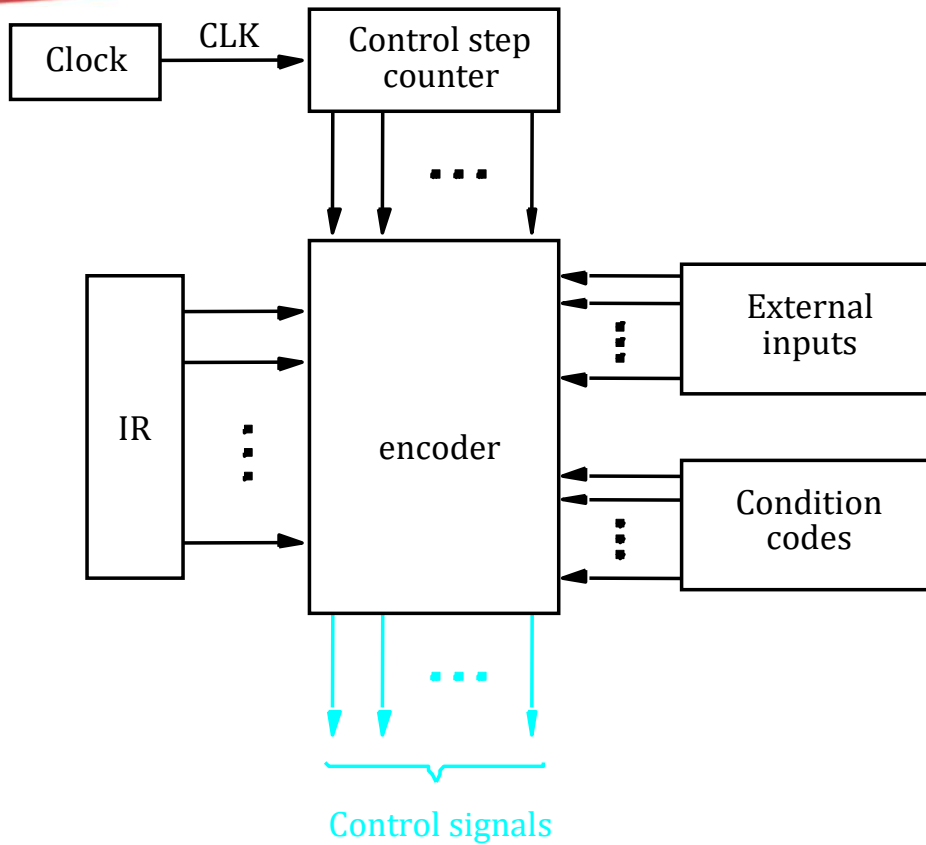
Recap the previous Class



Overview

- To execute instructions, the processor must have some means of **generating the control signals** needed in the proper sequence.
- Two categories: **hardwired control and microprogrammed control**
- Hardwired system can operate at **high speed**; but with **little flexibility**.

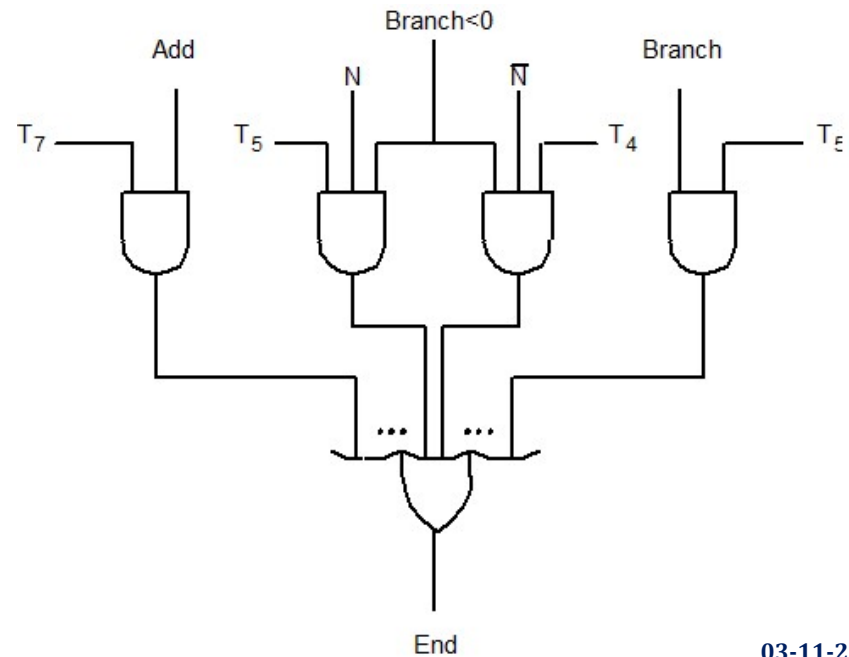
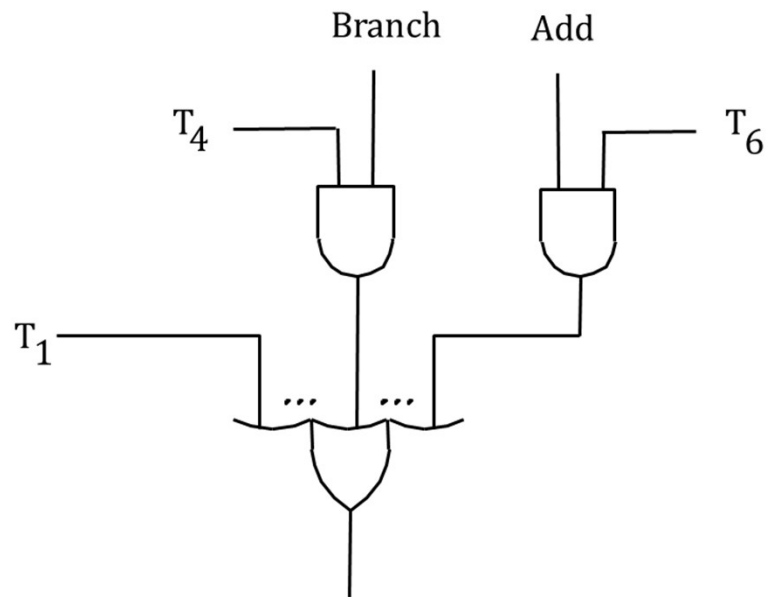
Control Unit Organization



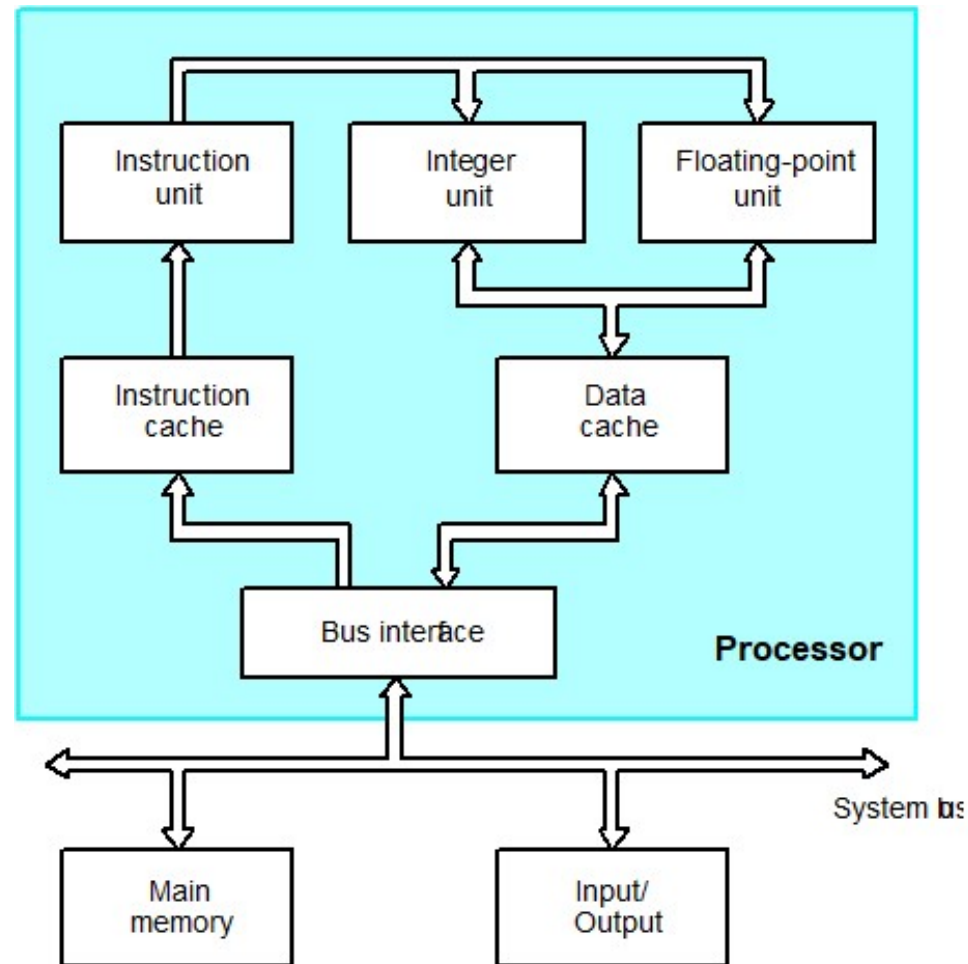
Generation of the Z_{in} and End control signal for the processor

$$Z_{in} = T_1 + T_6 \cdot \text{ADD} + T_4 \cdot \text{BR} + \dots$$

$$\text{End} = T_7 \cdot \text{ADD} + T_5 \cdot \text{BR} + (T_5 \cdot N + T_4 \cdot N) \cdot \text{BRN} + \dots$$



A Complete Processor





sns
INSTITUTIONS



Thank You