SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

19ECB202 – LINEAR AND DIGITAL CIRCUITS

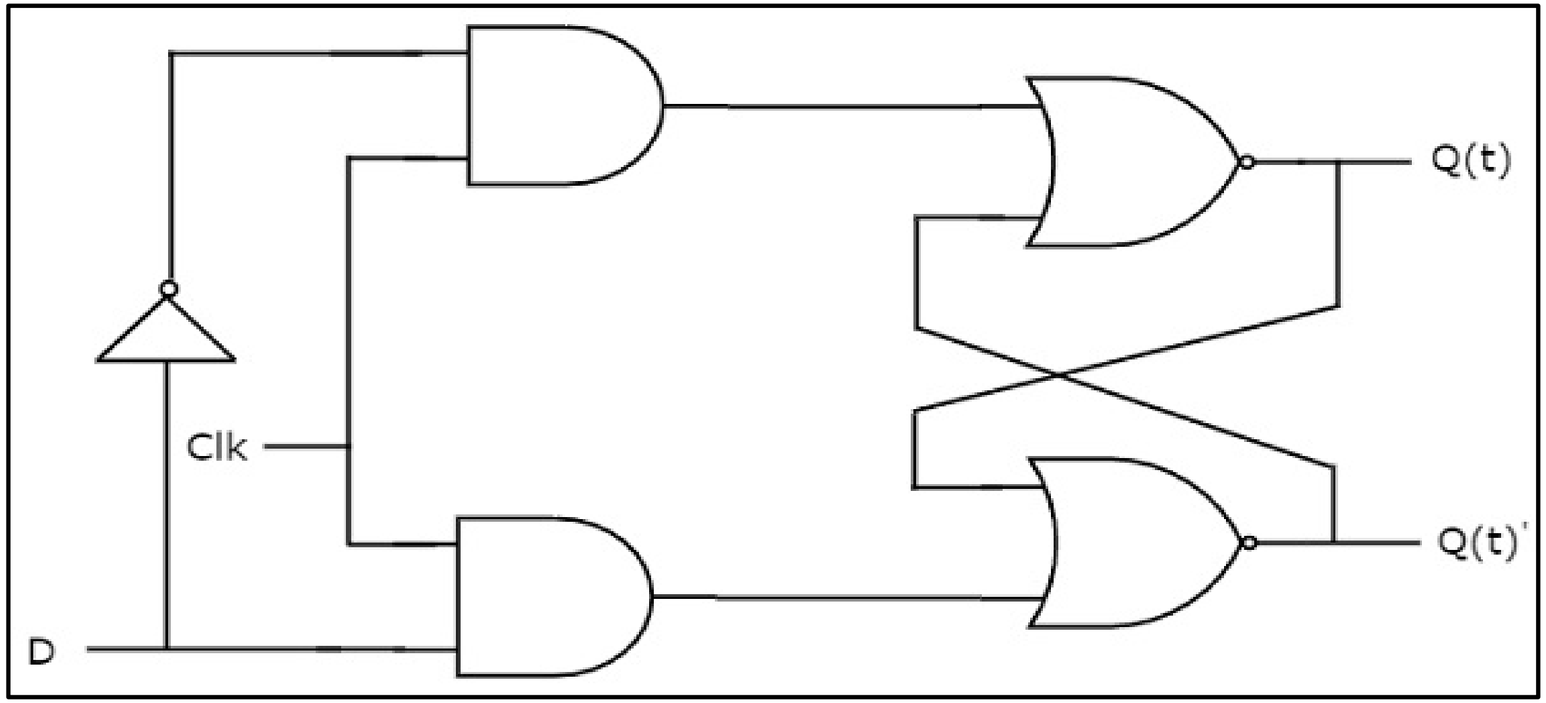
II YEAR/ III SEMESTER

UNIT 5 – SEQUENTIAL CIRCUITS

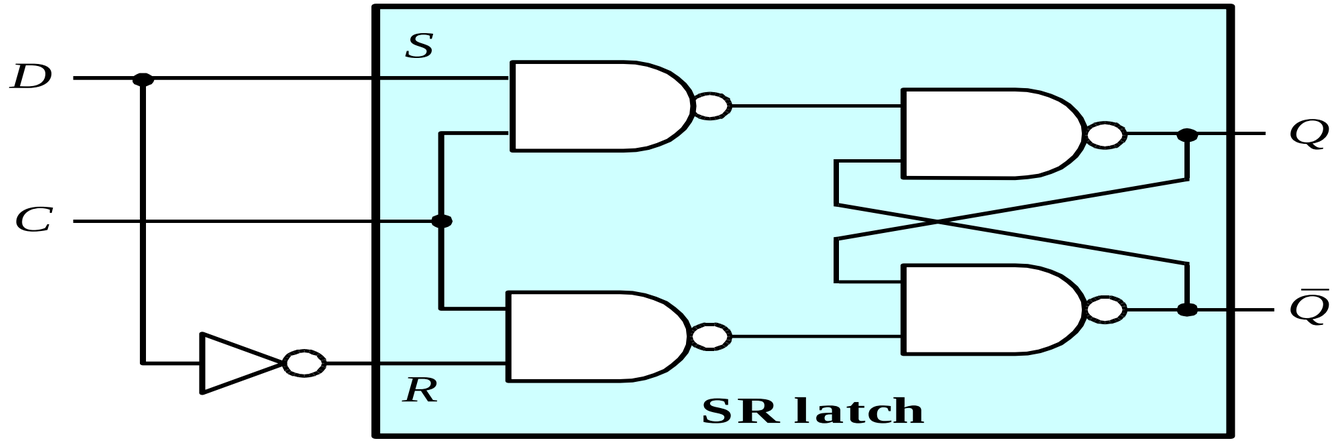
TOPIC 3 – D,T FLIP FLOPS, Master Slave

D Flip-Flop

D flip-flop operates with only positive clock transitions or negative clock transitions.
Whereas, D latch operates with enable signal.
That means, the output of D flip-flop is insensitive to the changes in the input, D except for active transition of the clock signal.



D Flip-Flop- Truth Table



(b)

C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state

D Flip-Flop- Working

- When storing data, a memory element's excitation input is simply the data to be stored.
- A device (which is called a delay latch or D latch) is needed that transfers a logic value on its excitation input D into the cross-coupled storage cell of a latch.
- The D latch can be created from a gated SR latch, by assigning S = D and R = D.

D Flip-Flop- Working

Characteristic equation:

- This equation can be derived from that of the gated SR latch by substituting D for S and D for R:

  $Q^* = DC + CQ$

- When the enable signal is low, (C = 0), the equation reduces to

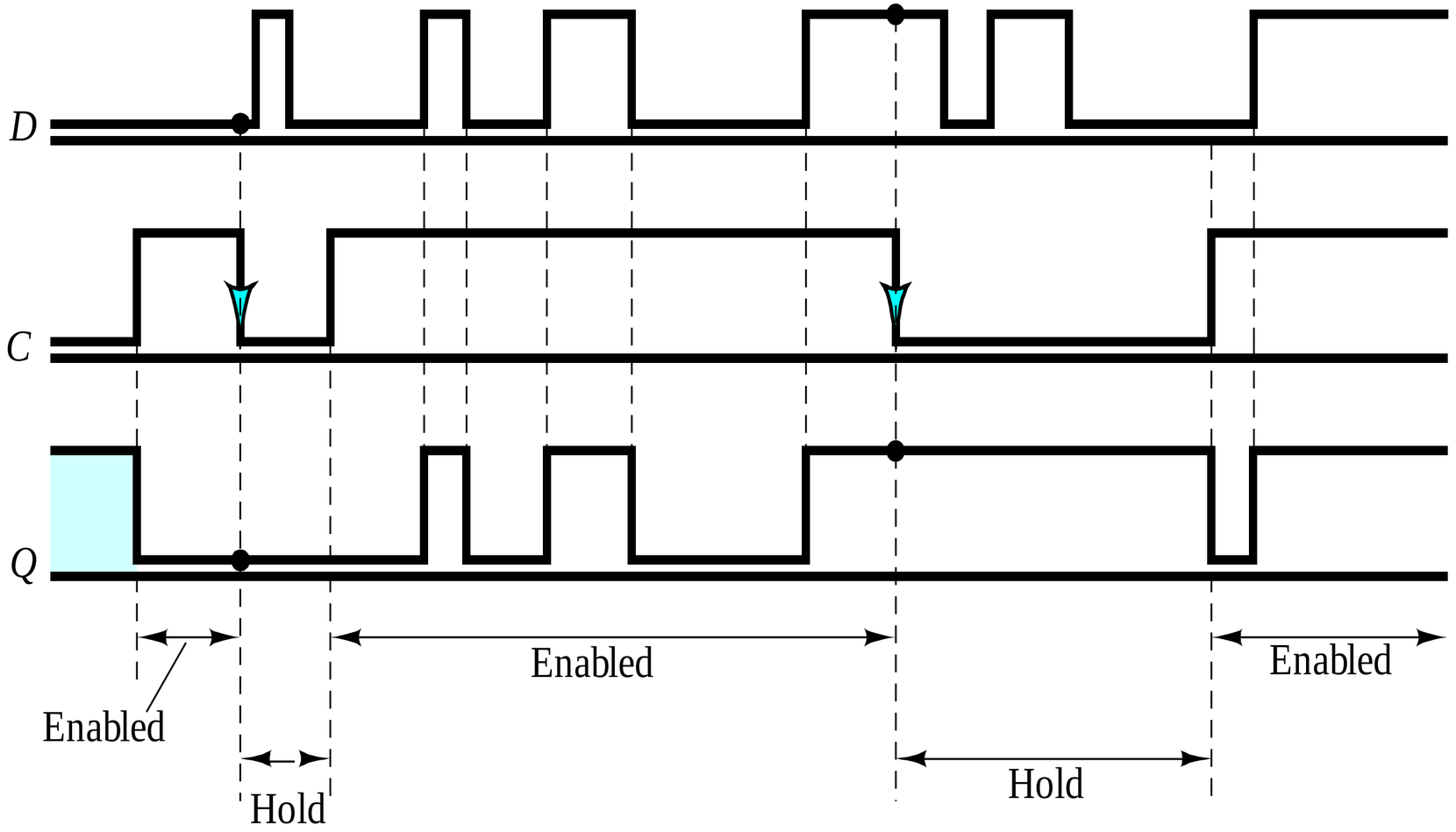
  $Q^* = Q$, the latch is placed in hold mode (no change)

  operating mode with the latch holding the last value of D that was entered

- When the enable signal is high (C = 1),

  $Q^* = D$, the excitation input D is gated directly to output Q (gated or enabled mode).

D Flip-Flop- Timing Diagram

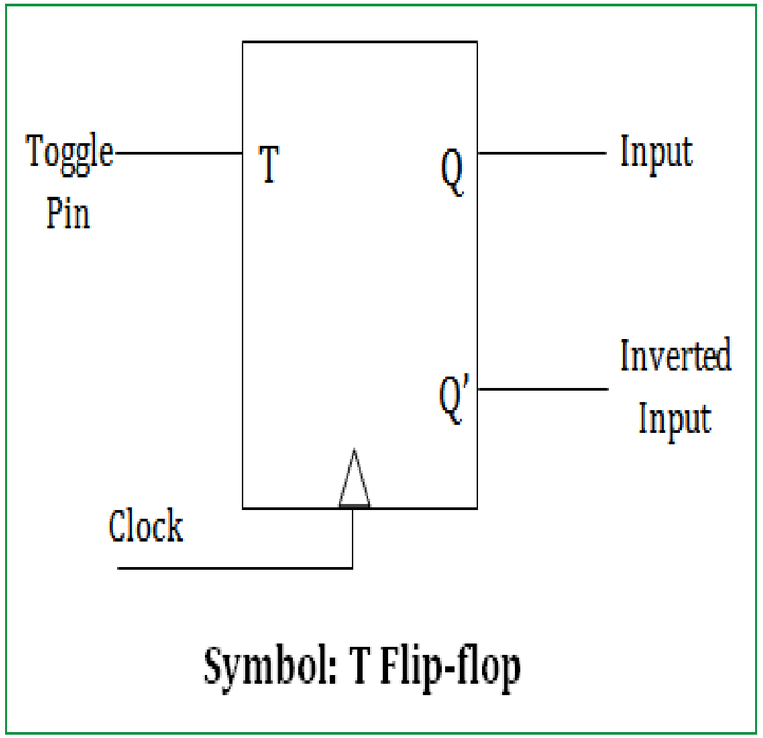


T Flip-Flop

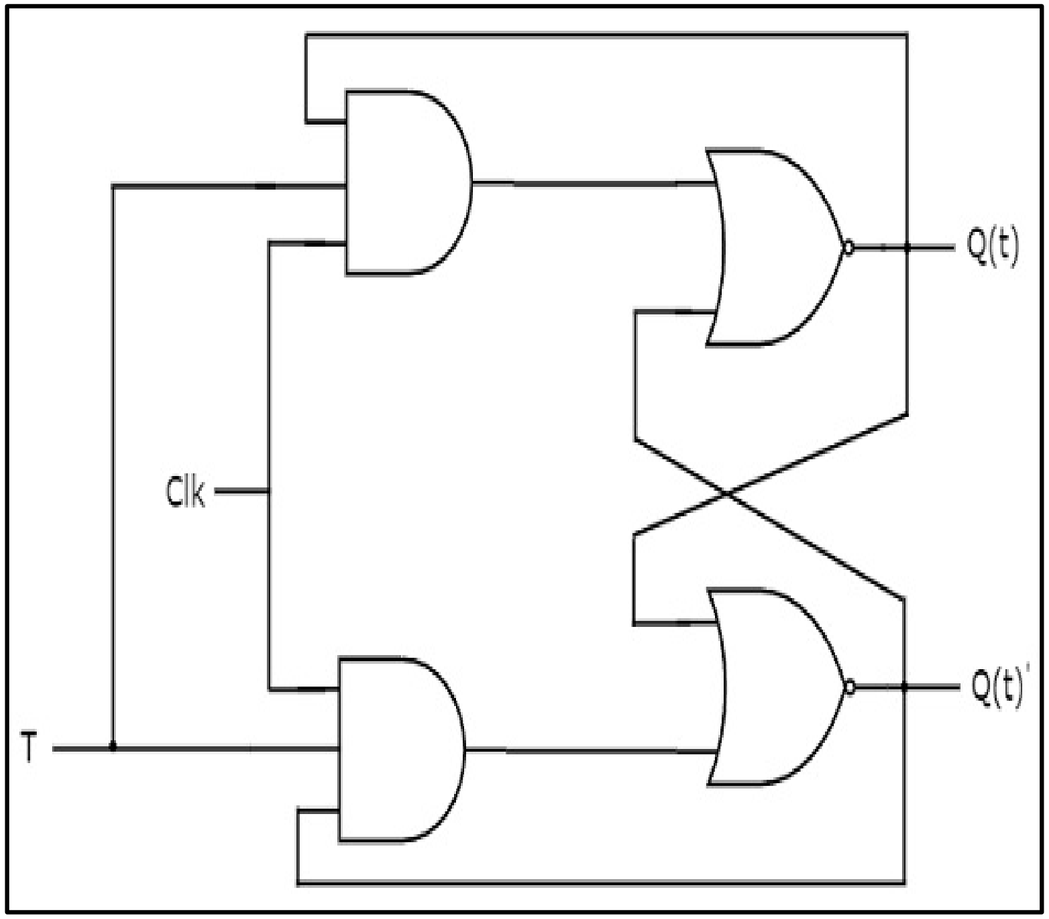
- T flip-flop is the simplified version of JK flip-flop.
- It is obtained by connecting the same input ‘T’ to both inputs of JK flip-flop.
- It operates with only positive clock transitions or negative clock transitions.

- The name T flip-flop is termed from the nature of toggling operation
- The major applications of T flip-flop are counters and control circuits
- T flip flop is modified form of JK flip-flop making it to operate in toggling region
- Whenever the clock signal is LOW, the input is never going to affect the output state

T Flip-Flop



Symbol: T Flip-flop



T Flip-Flop- Truth Table

	Previous		Next	
T	Q_{Prev}	Q'_{Prev}	Q_{Next}	Q'_{Next}
0	0	1	0	1
0	1	0	1	0
1	0	1	1	0
1	1	0	0	1

T Flip-Flop- Truth Table

➢When the T input is low, then the next sate of the T flip flop is same as the present state.

•T = 0 and present state = 0 then the next state = 0

•T = 0 and present state = 1 then the next state = 1

➢When the T input is high and during the positive transition of the clock signal, the next state of the T flip –flop is the inverse of present state.

•T = 1 and present state = 0 then the next state = 1

•T = 1 and present state = 1 then the next state = 0

Applications

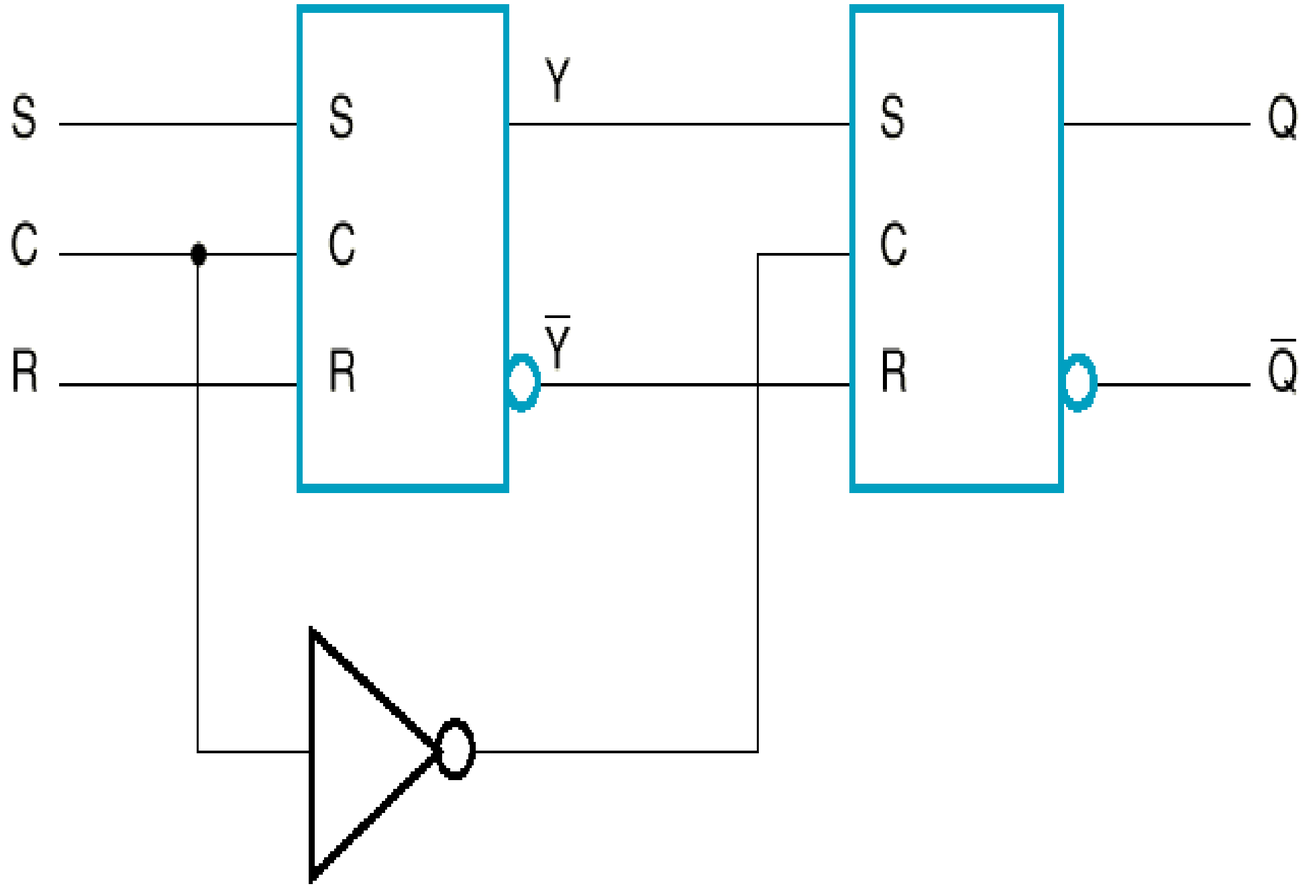
➢Frequency Division Circuits.

➢2 –Bit Parallel Load Registers.

T Flip-Flop- Characteristic Table & Equation

T flip-flop		
Q(t)	Q(t+1)	DR
0	0	0
0	1	1
1	0	1
1	1	0

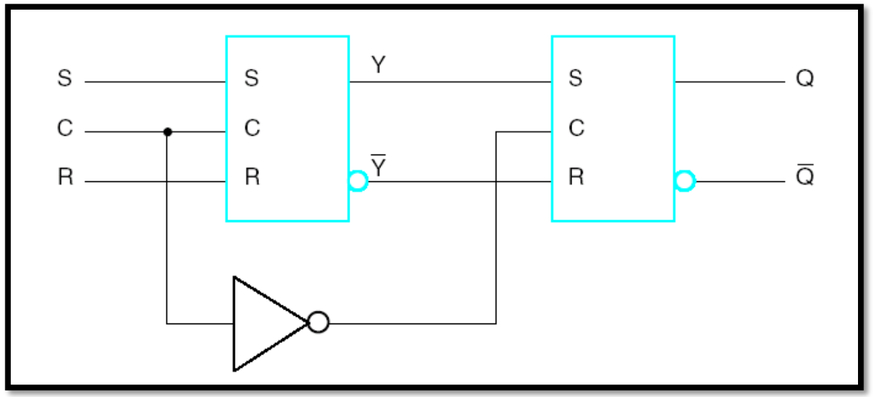
Master-Slave FF configuration using SR latches



Master-Slave FF configuration using SR latches

S	R	CLK	Q	Q'	
0	0	1	Q_0	Q_0'	Store
0	1	1	0	1	Reset
1	0	1	1	0	Set
1	1	1	1	1	Disallowed
X	X	0	Q_0	Q_0'	Store

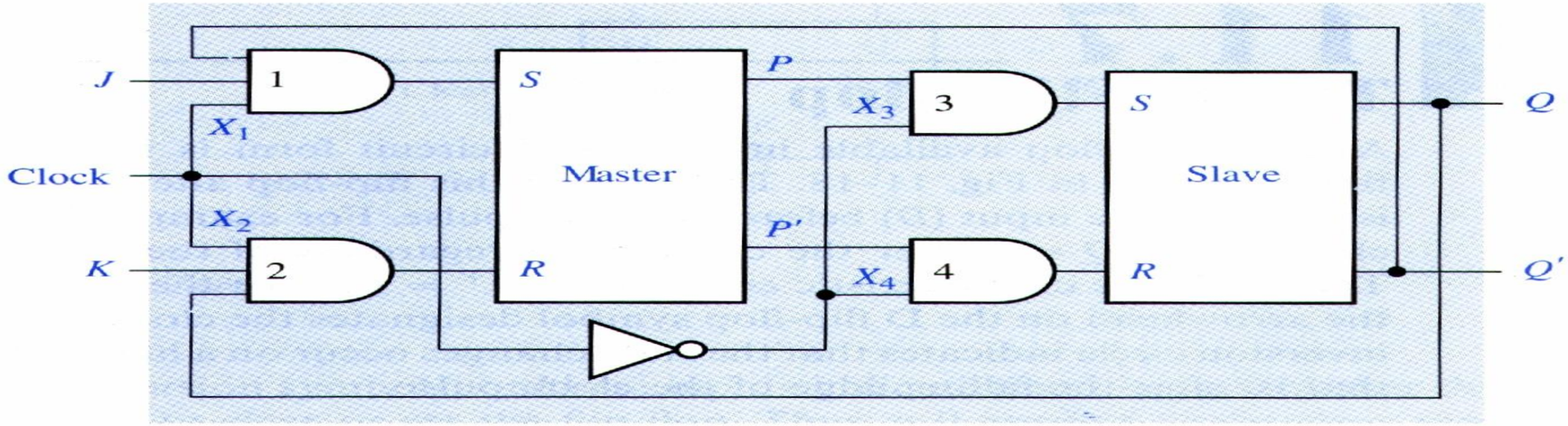
- When C=1, master is enabled and stores *new* data, slave stores *old* data.
- When C=0, master's state passes to enabled slave, master not sensitive to new data (disabled).



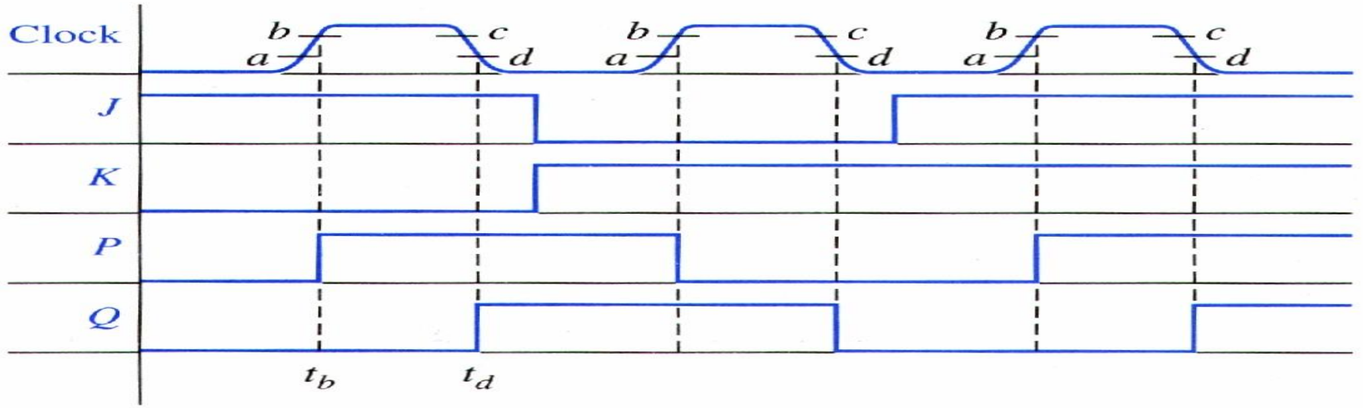
MASTER SLAVE J K Flip flop

- Clocked J-K FF (falling edge)
  - Realization using two S-R latches
  - Note where J and K change.
  - One flip-flop acts as the “Master” circuit, which triggers on the leading edge of the clock pulse
  - while the other acts as the “Slave” circuit, which triggers on the falling edge of the clock pulse.
  - This results in the two sections, the master section and the slave section being enabled during opposite half-cycles of the clock signal.
  - The slave section being enabled during opposite half-cycles of the clock signal.

MASTER SLAVE J K Flip flop



(a) Master-slave J-K flip-flop



(b) Internal timing diagram for master-slave J-K flip-flop

Excitation Tables

SR Flip-flop			
Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D Flip-flop		
Q(t)	Q(t+1)	DR
0	0	0
0	1	1
1	0	0
1	1	1

JK flip-flop			
Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

T flip-flop		
Q(t)	Q(t+1)	DR
0	0	0
0	1	1
1	0	1
1	1	0

THANK YOU