SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

19ECB202 – LINEAR AND DIGITAL CIRCUITS

II YEAR/ III SEMESTER

UNIT 5 – SEQUENTIAL CIRCUITS and PLC

TOPIC 2 – FLIP FLOPS- JK

Flip Flops

•The basic S-R NAND flip-flop circuit has many advantages and uses in sequential logic circuits but it suffers from two basic switching problems.

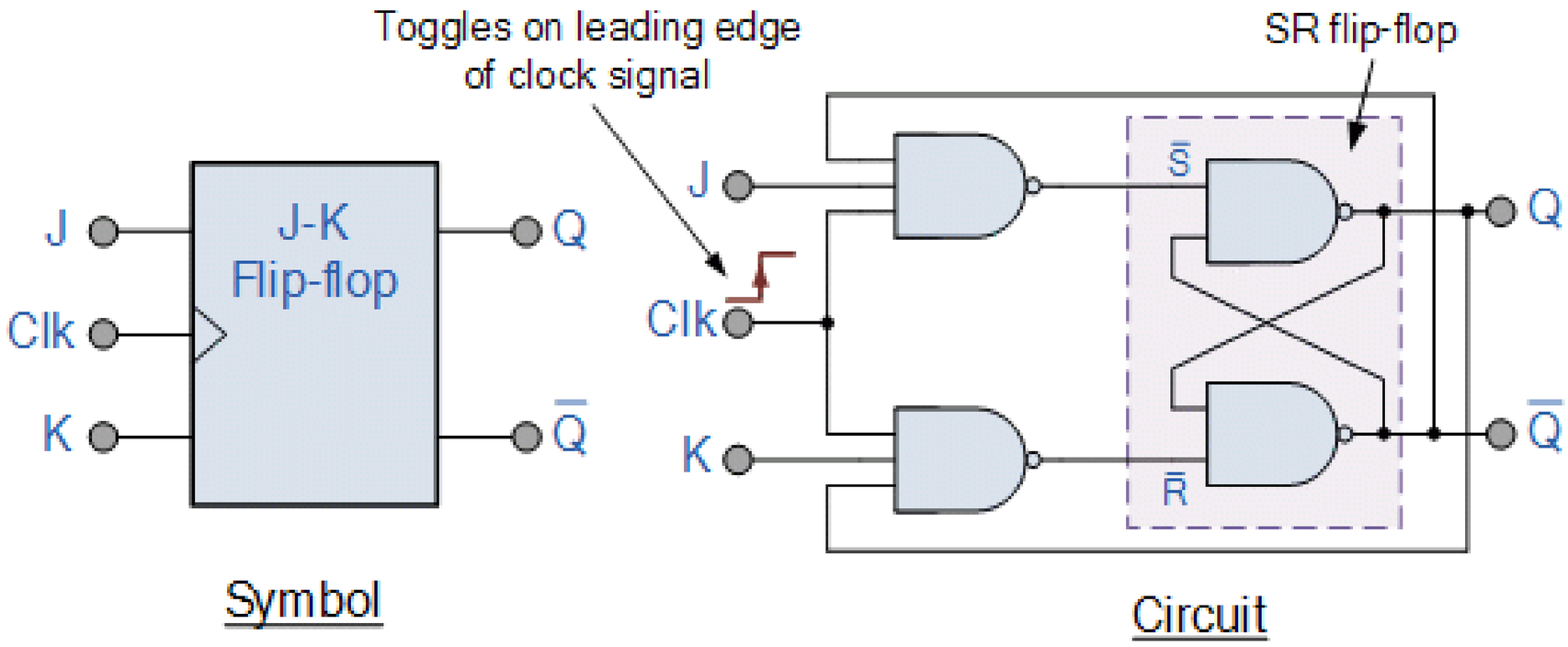
1. The Set = 0 and Reset = 0 condition (S = R = 0) must always be avoided
2. If Set or Reset change state while the enable (EN) input is high the correct latching action may not occur

•Then to overcome these two fundamental design problems with the SR flip-flop design, the **JK flip Flop** was developed.

•The two inputs labelled “J” and “K” are autonomous letters chosen by its inventor Jack Kilby to distinguish the flip-flop design from other types.

JK Flip Flop

JK flip-flop is the modified version of SR flip-flop. It operates with only positive clock transitions or negative clock transitions.



JK Flip Flop

- The **JK flip flop** is basically a gated SR flip-flop with the addition of a clock input circuitry
- It prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”.
- Due to this additional clocked input, a JK flip-flop has four possible input combinations, “logic 1”, “logic 0”, “no change” and “toggle”.

JK Flip Flop Truth Table

J	K	Q $t+1$
0	0	Q t
0	1	0
1	0	1
1	1	Q t '

JK Flip Flop Truth Table

	Clock	Input		Output		Description
	Clk	J	K	Q	Q	
for the SR Latch	X	0	0	1	0	Memory no change
	X	0	0	0	1	
	¯↓_	0	1	1	0	Reset Q » 0
	X	0	1	0	1	
	¯↓_	1	0	0	1	Set Q » 1
	X	1	0	1	0	
toggle action	¯↓_	1	1	0	1	Toggle
	¯↓_	1	1	1	0	

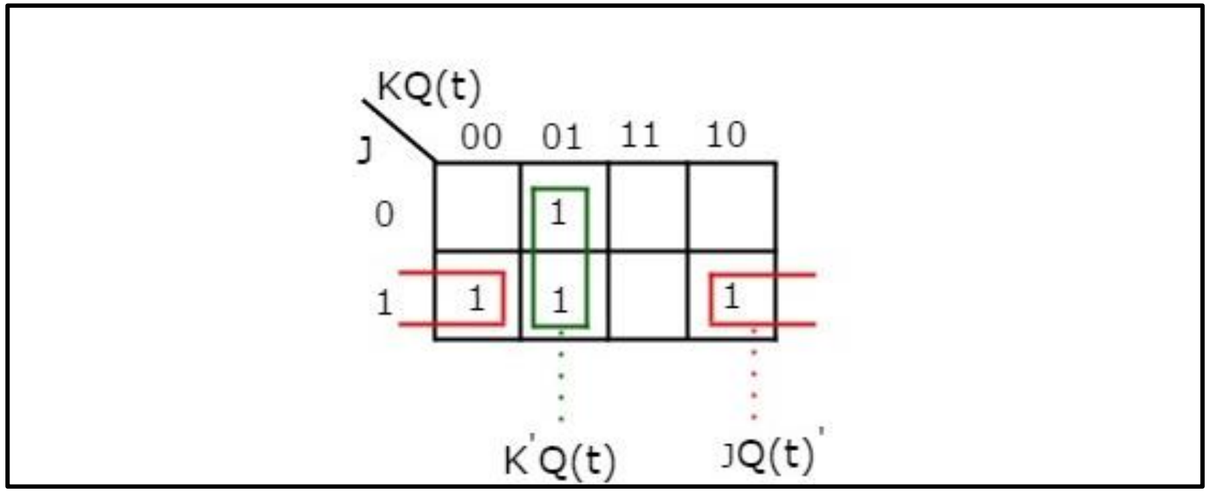
JK Flip Flop Truth Table

- If the circuit is now “SET” the J input is inhibited by the “0” status of $\overline{Q}$ through the lower NAND gate.
- If the circuit is “RESET” the K input is inhibited by the “0” status of Q through the upper NAND gate.
- As Q and $\overline{Q}$ are always different ,It can be used to control the input.
- When both inputs J and K are equal to logic “1”, the JK flip flop toggles

JK Flip Flop Truth Table

INPUTS			OUTPUTS	REMARKS
J	**K**	**Q_n (Present State)**	**Q_{n+1} (Next State)**	**States and Conditions**
0	0	X	Q_n	Hold State condition J = K = 0
0	1	X	0	Reset state condition J = 0 , K = 1
1	0	X	1	Set state condition J = 1 , K = 0
1	1	X	Q'_n	Toggle state condition J = K = 1

JK Flip Flop Characteristic Equation

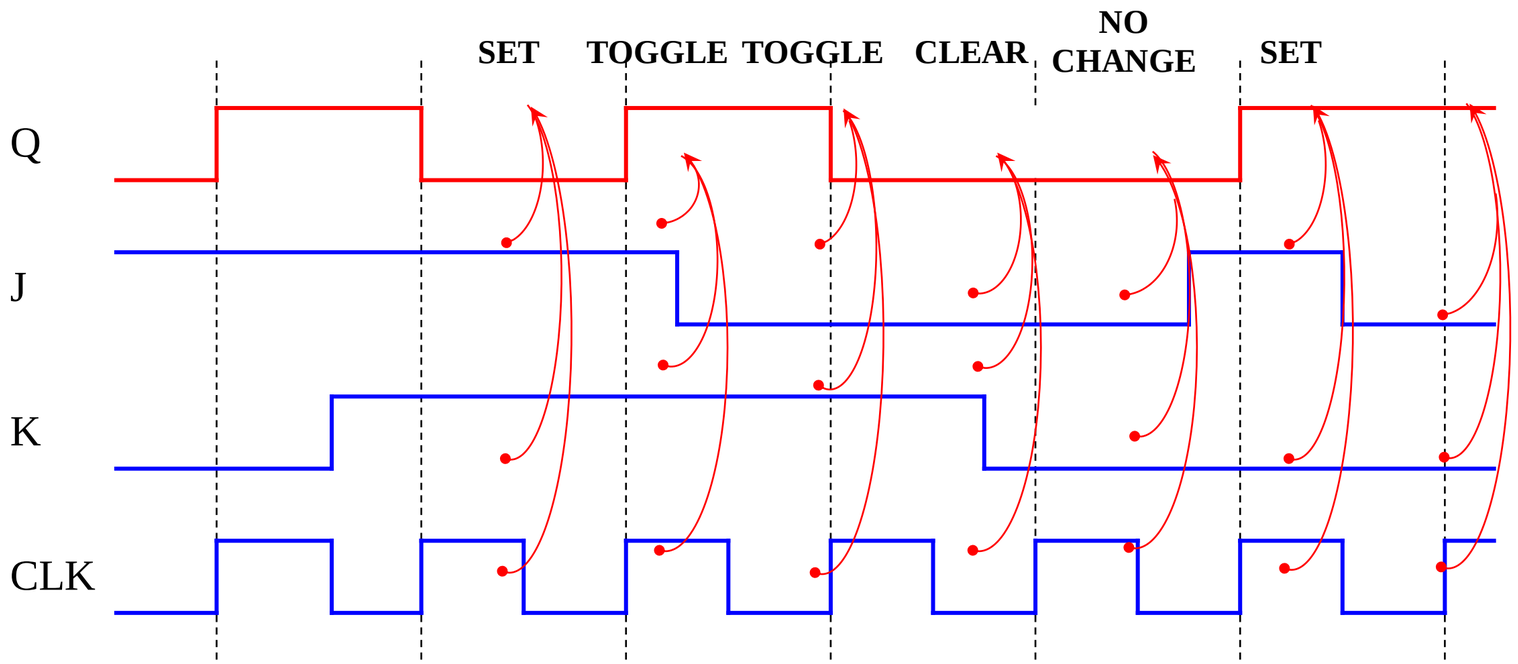


$$Q(t+1) = JQ(t)' + K'Q(t)$$

JK Flip Flop Excitation Table

JK flip-flop			
Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

JK Flip Flop Timing diagram



SR Vs JK Flip Flop

- Both JK flip flop and SR flip flop are functionally same.

  The difference between them is-

- In JK flip flop, indeterminate state does not occur.
- In JK flip flop, instead of indeterminate state, the present state toggles.
- The present state gets inverted when both the inputs are 1.