SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

19ECB202 – LINEAR AND DIGITAL CIRCUITS

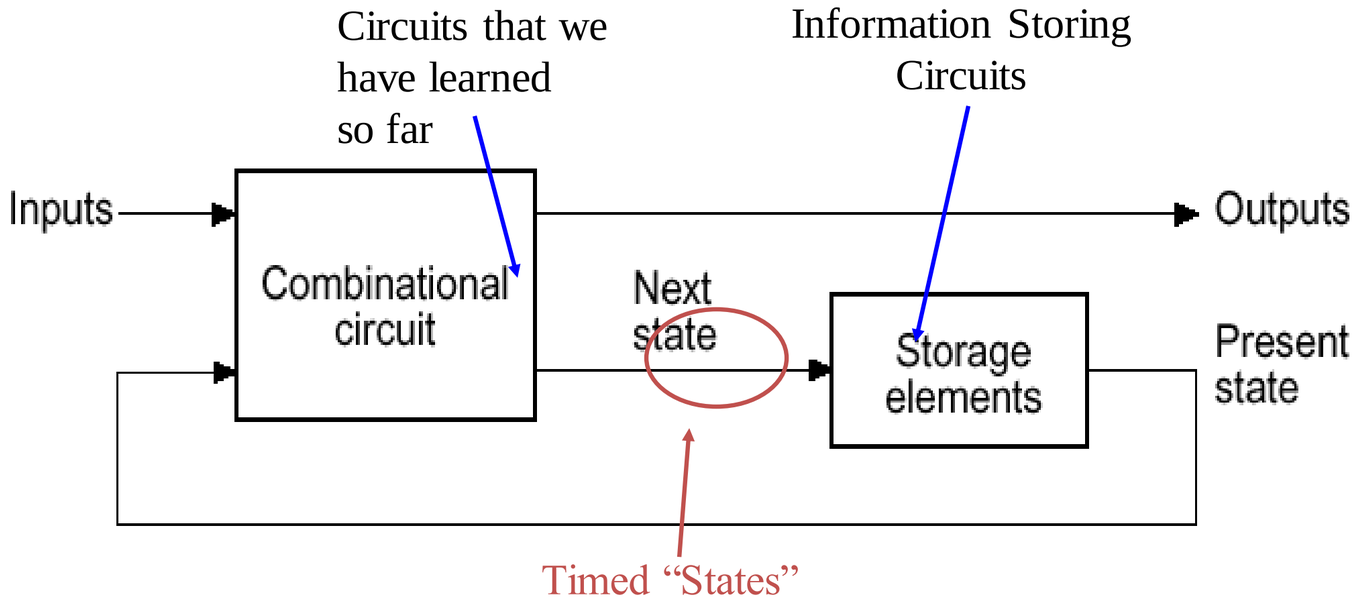
II YEAR/ III SEMESTER

UNIT 5 – SEQUENTIAL CIRCUITS and PLC

TOPIC 1 – FLIP FLOP FUNDAMENTALS and SR Flipflop

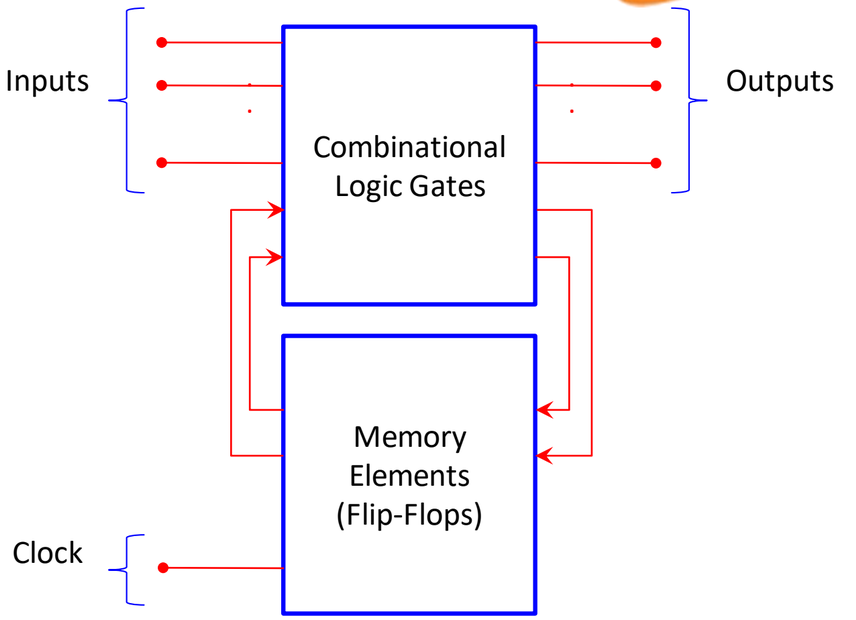
Sequential Circuits

- Sequential Logic:
  - Output depends not only on current input but also on past input values, e.g., design a counter
  - Need some type of memory to remember the past input values



Sequential Circuits

- Sequential Logic circuits remember past inputs and past circuit state.
- Outputs from the system are “fed back” as new inputs
  - With gate delay and wire delay
- The storage elements are circuits that are capable of storing binary information: memory.



There are two types of sequential circuits:

- **Synchronous sequential circuit:** circuit output changes only at some discrete instants of time. This type of circuits achieves synchronization by using a timing signal called the clock.
- **Asynchronous sequential circuit:** circuit output can change at any time (clockless).

Flip Flops

- In electronics a flip-flop or latch is a circuit that has two stable states and can be used to store state information –a bistable multivibrator.
- The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs.
- Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.
- Flip-flops and latches are used as data storage elements.
- A flip-flop is a device which stores a single bit(binary digit) of data; one of its two states represents a "one" and the other represents a “zero”.

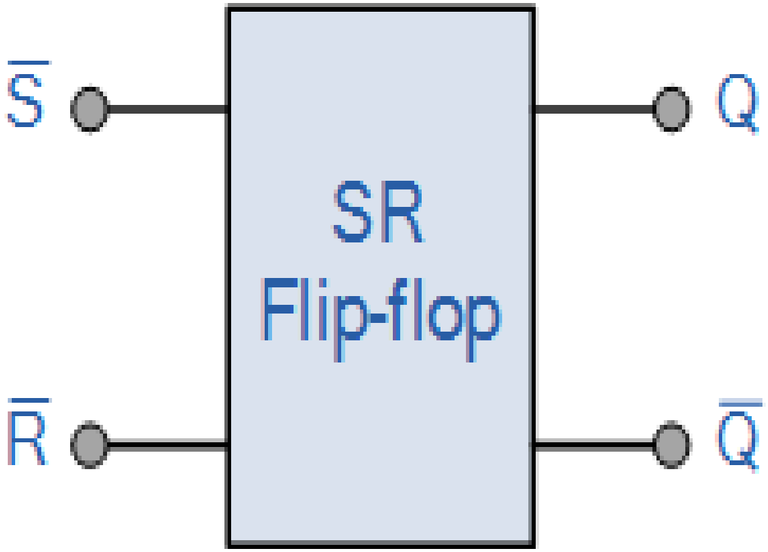
Flip Flops

- Flip flop is a sequential circuit
- It samples its inputs and changes its outputs only at particular instants of time and not continuously.
- Flip flop is said to be edge sensitive or edge triggered rather than being level triggered like latches

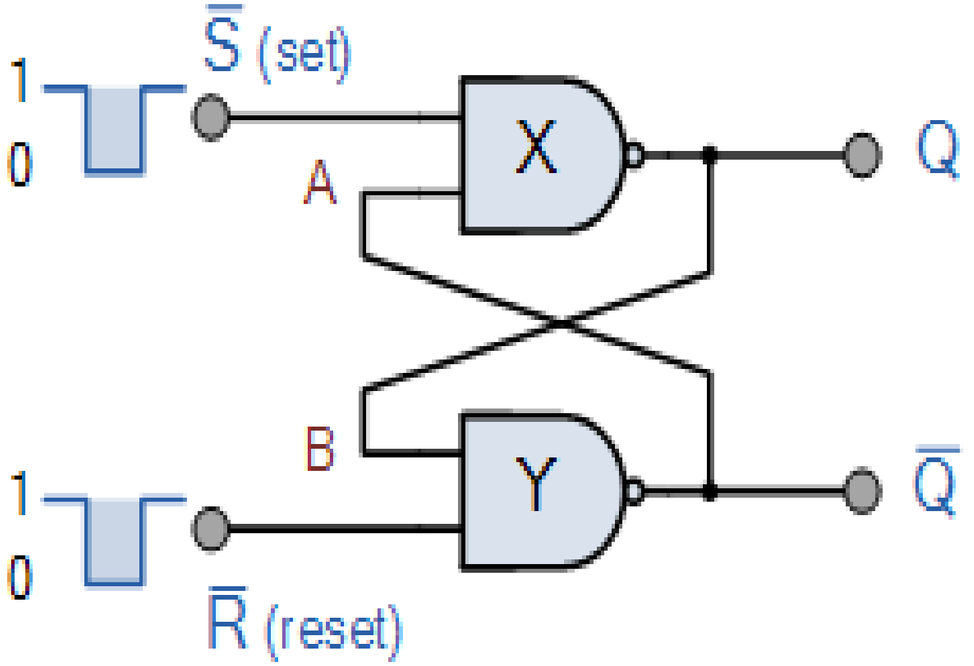
TYPES

- SR Flip-Flop
- D Flip-Flop
- JK Flip-Flop
- T Flip-Flop

SR Flip Flop



Symbol



Circuit

SR Flip Flop

The Set State

- If the input R is at logic level “0” (R = 0) & S is at logic level “1” (S = 1)
  Its output Q must be at a logic level “1” .
- Output $\overline{Q}$ is also fed back to input “A”
  - Both inputs to NAND gate *X* are at logic level “1”
  - Its output Q must be at logic level “0”.

- If the reset input R changes state, and goes HIGH to logic “1” with S remaining HIGH also at logic level “1”
  - NAND gate *Y* inputs are now R = “1” and B = “0”.
  - Since one of its inputs is still at logic level “0” the output at $\overline{Q}$ still remains HIGH at logic level “1” and there is no change of state.
  - Therefore, the flip-flop circuit is said to be “Latched” or “Set” with $\overline{Q}$ = “1” and Q = “0”.

SR Flip Flop

Reset State

- $\overline{Q}$ is at logic level "0", its inverse output at Q is at logic level "1"
  Given by R = "1" and S = "0".

- As gate *X* has one of its inputs at logic "0" its output Q must equal logic level "1"
  Output Q is fed back to input "B", so both inputs to NAND gate *Y* are at logic "1", therefore, $\overline{Q}$ = "0".

- If the set input, S now changes state to logic "1" with input R remaining at logic "1"
  - output $\overline{Q}$ still remains LOW at logic level "0" and there is no change of state.

- Therefore, the flip-flop circuits "Reset" state has also been latched

SR Flip Flop Truth Table

S-R flip flop behavior

Present state

The state of Q output at the time the input signals are applied.

Next state

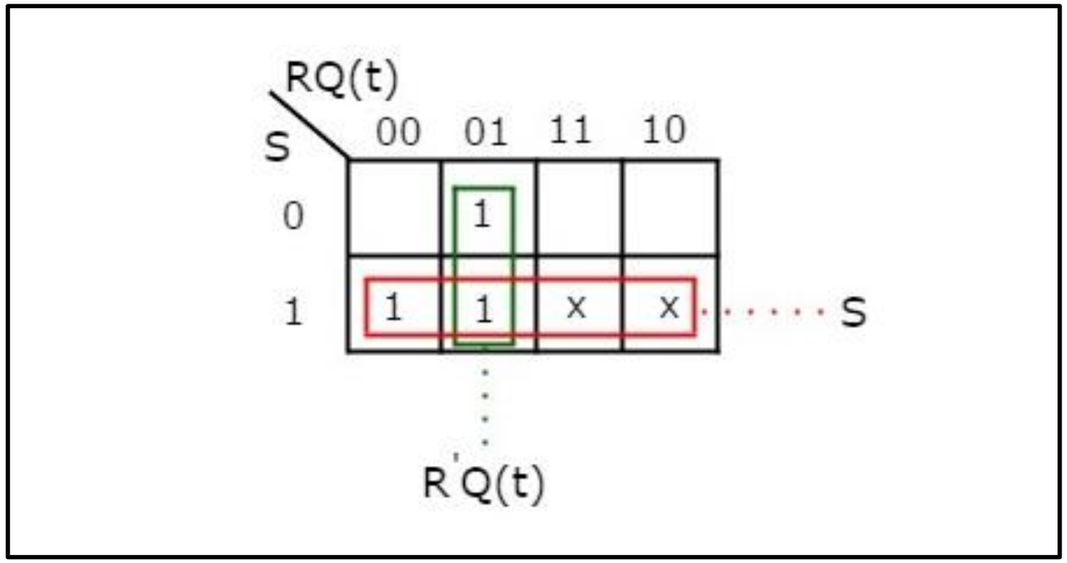
The state of Q output after the flipflop has reacted to the input signals.

State	S	R	Q	$\overline{Q}$	Description
Set	1	0	0	1	Set $\overline{Q}$ » 1
	1	1	0	1	no change
Reset	0	1	1	0	Reset $\overline{Q}$ » 0
	1	1	1	0	no change
Invalid	0	0	1	1	Invalid Condition

SR Flip Flop Truth Table

- When both inputs S = “1” and R = “1” the outputs Q and $\overline{Q}$ can be at either logic level “1” or “0”, depending upon the state of the inputs S or R BEFORE this input condition existed.
- Therefore the condition of S = R = “1” does not change the state of the outputs Q and $\overline{Q}$.
- The input state of S = “0” and R = “0” is an undesirable or invalid condition
- The condition of S = R = “0” causes both outputs Q and $\overline{Q}$ to be HIGH together at logic level “1”
- The result is that the flip-flop looses control of Q and $\overline{Q}$
- The flip-flop becomes unstable and switches to an unknown data state based upon the unbalance

SR Flip Flop Characteristic Equation



$$Q(t+1) = S + R'Q(t)$$

SR Flip Flop Switching Diagram