



SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution



Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++'
Grade

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

16EC303–VLSI DESIGN

III YEAR/₁ V SEMESTER

UNIT 4 –VLSI TESTING

TOPIC 5: Design Strategies -BIST & BOUNDARY SCAN



OUTLINE



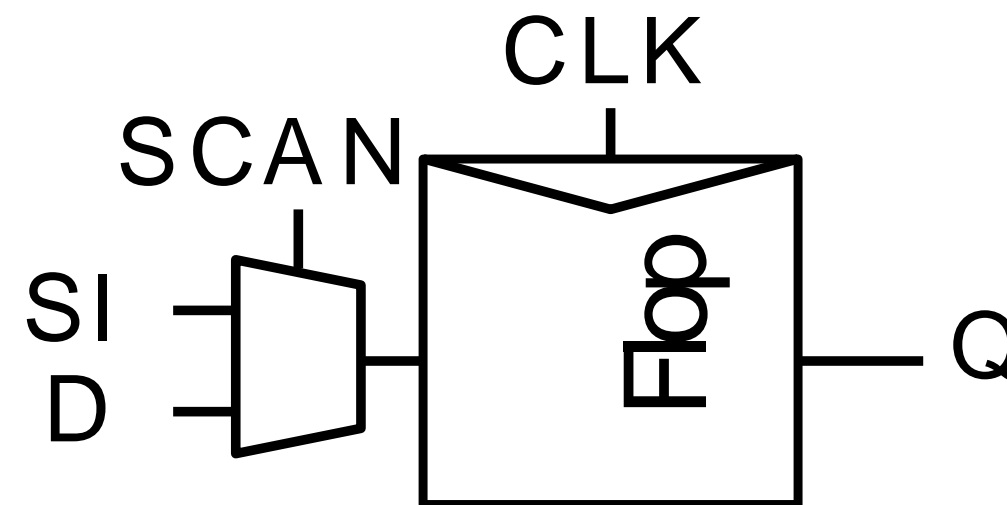
- Design for Test
 - Scan-FLIPFLOP
 - BIST
 - PRSG
 - BILBOActivity
- Boundary Scan
 - Examples
 - Interfacesummary



DESIGN FOR TEST



- Design the chip to increase observability and controllability
- If each register could be observed and controlled, test problem reduces to testing combinational logic between registers.
- Better yet, logic blocks could enter test mode where they generate test patterns and report the results automatically.

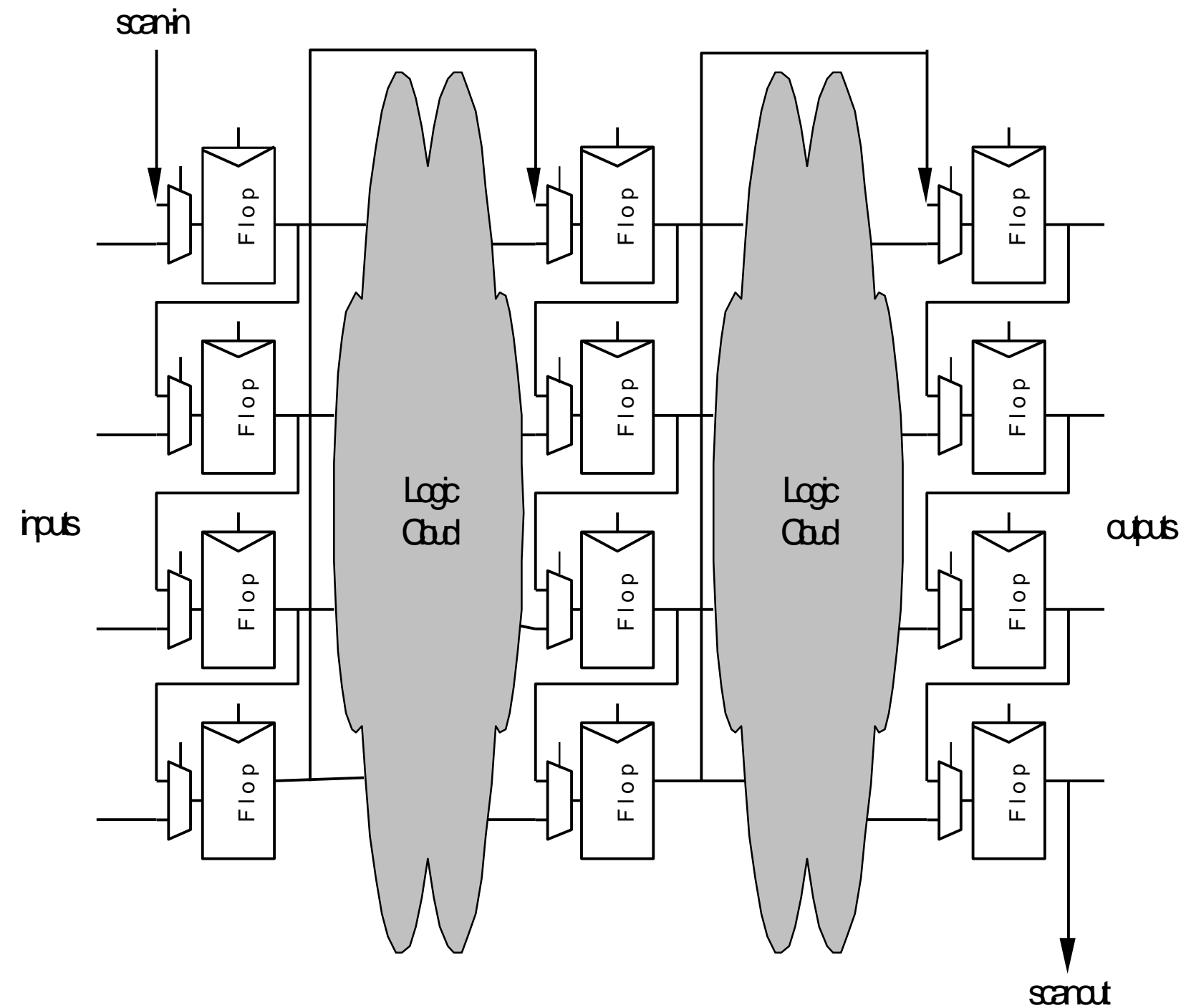




SCAN

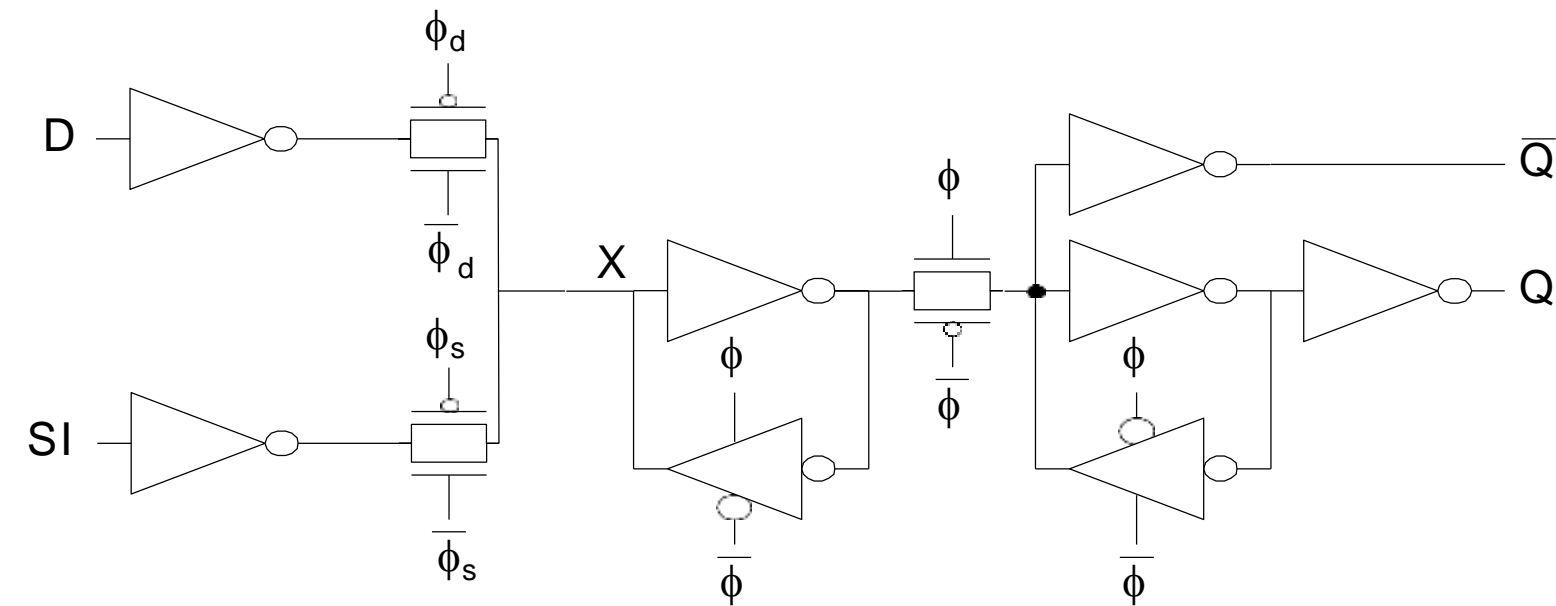
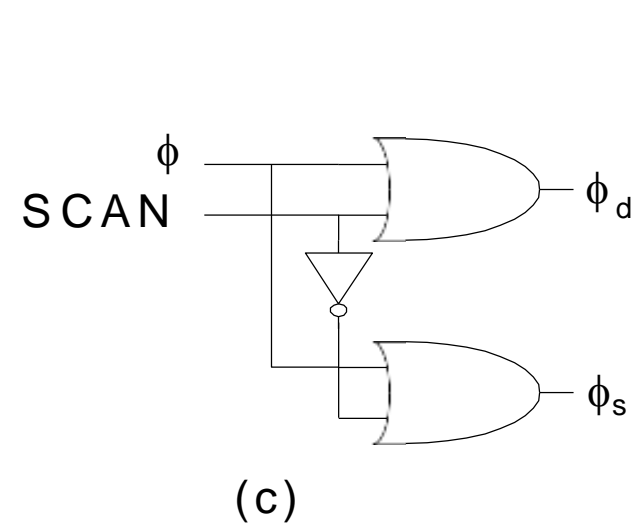
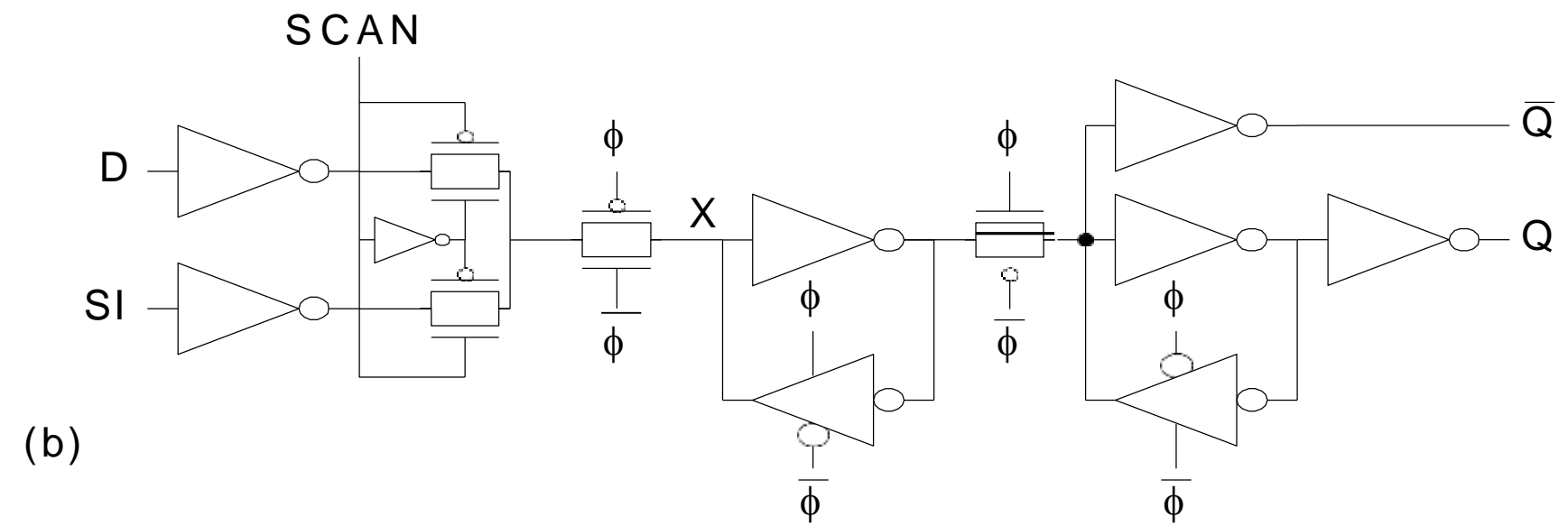
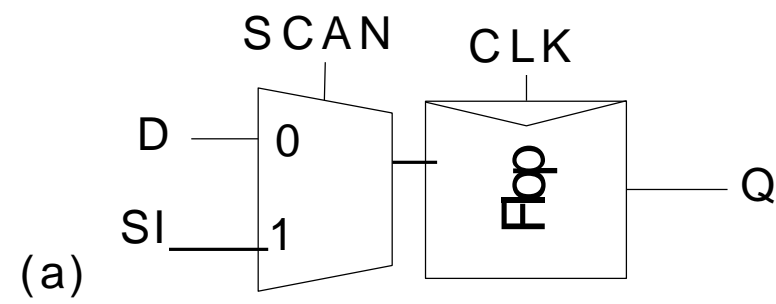


- Convert each flip-flop to a scan register
 - Only costs one extra multiplexer
- Normal mode: flip-flops behave as usual
- Scan mode: shift register
- Contents of flops can be scanned out and new values scanned in





SCANNABLE FLIP-FLOPS



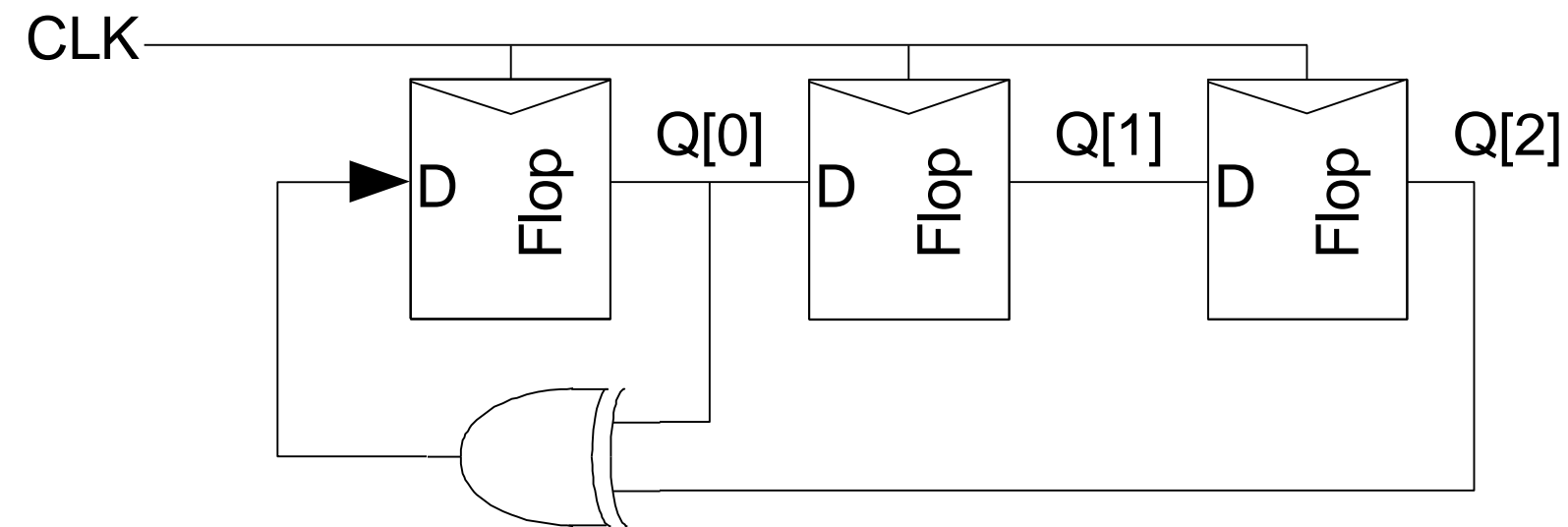


BUILT-IN SELF-TEST



Built-in self-test lets blocks test themselves

Generate pseudo-random inputs to comb. Logic. Combine outputs into a syndrome With high probability, block is fault-free if it produces the expected syndrome.





PRSG



- Linear Feedback Shift Register
 - Shift register with input taken from XOR of state
 - Pseudo-Random Sequence Generator

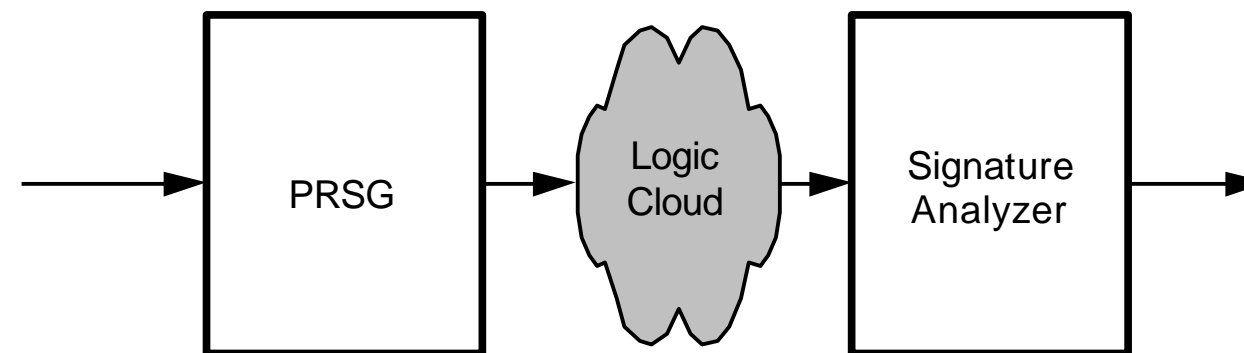
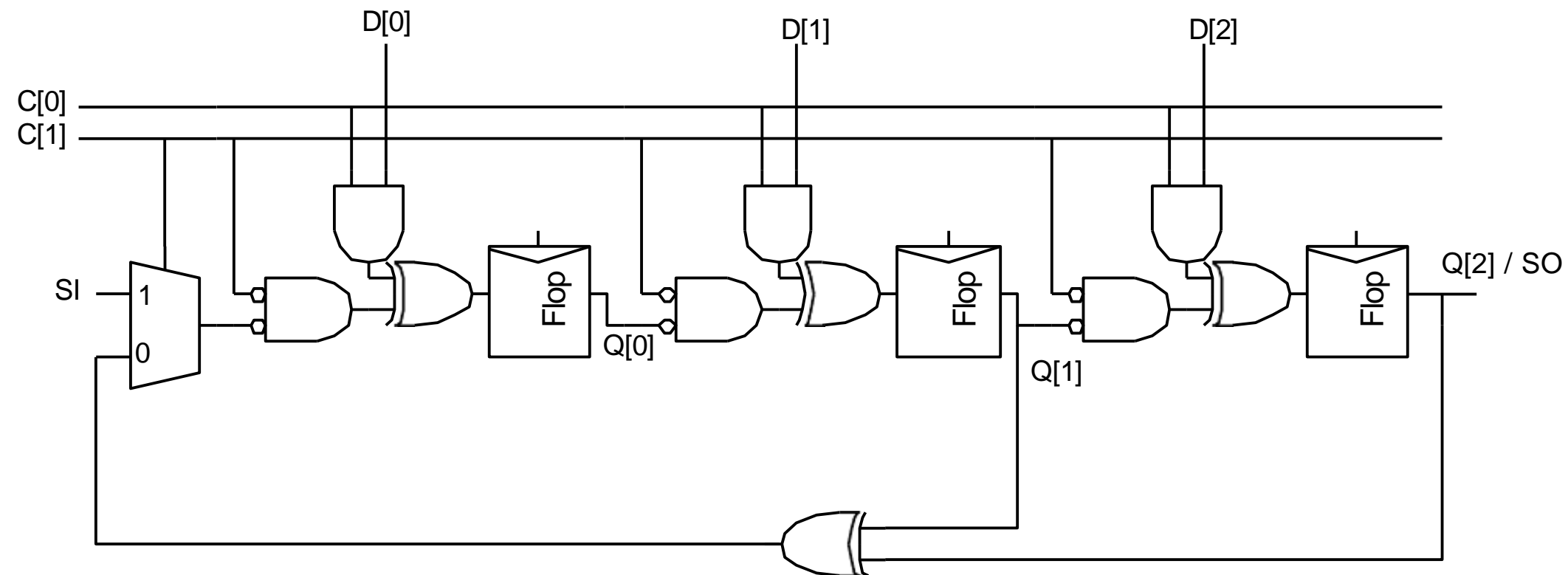
Step	Q
0	111
1	110
2	101
3	010
4	100
5	001
6	011
7	111 (repeats)



BILBO



- Built-in Logic Block Observer
 - Combine scan with PRSG & signature analysis



MODE	C[1]	C[0]
Scan	0	0
Test	0	1
Reset	1	0
Normal	1	1



ACTIVITY



DEBATE: BOYS VS GIRLS



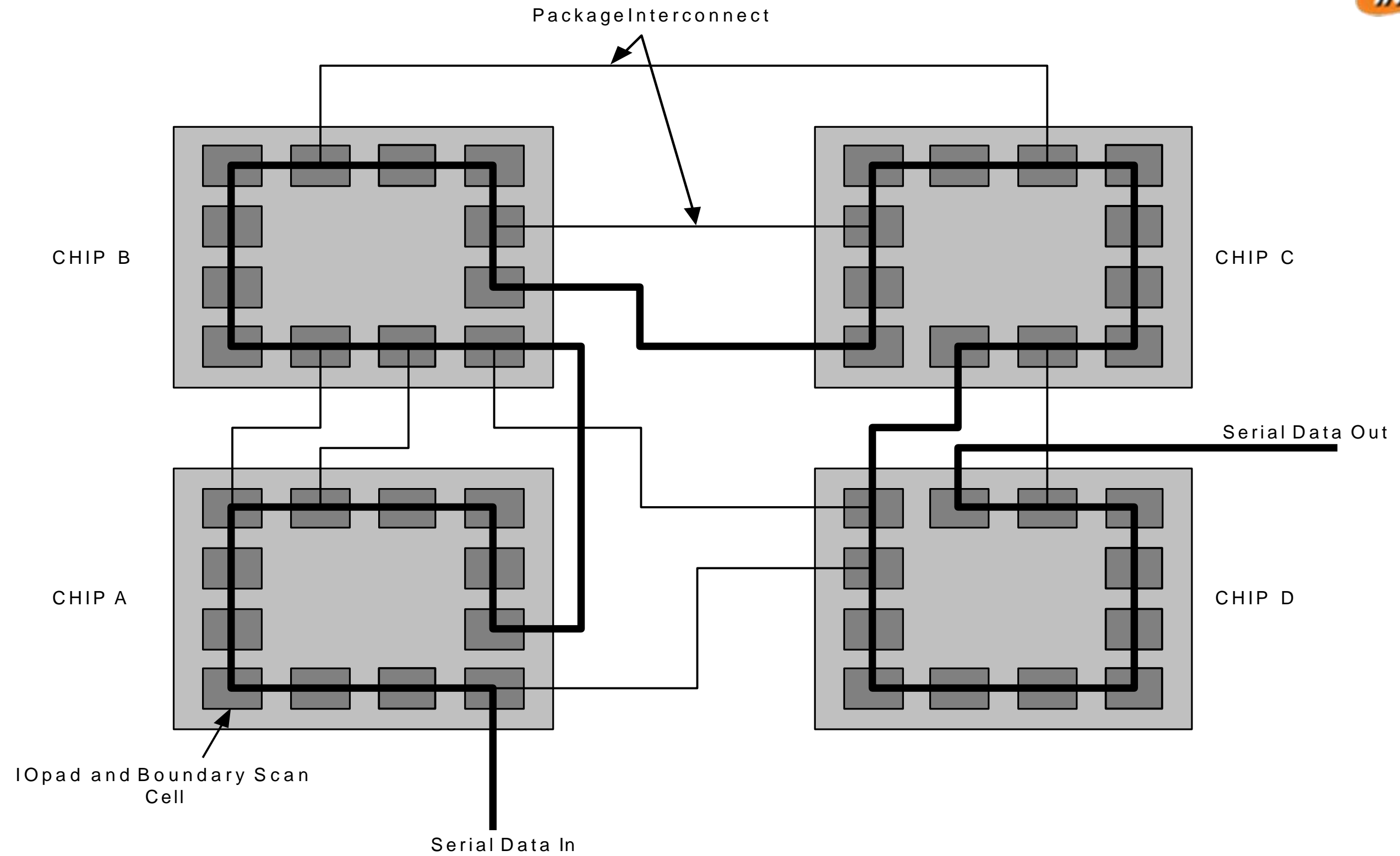
BOUNDARY SCAN



- Testing boards is also difficult
 - Need to verify solder joints are good
 - Drive a pin to 0, then to 1
 - Check that all connected pins get the values
- Through-hole boards used “bed of nails”
- SMT and BGA boards cannot easily contact pins
- Build capability of observing and controlling pins into each chip to make board test easier



BOUNDARY SCAN EXAMPLE





BOUNDARY SCAN INTERFACE

Boundary scan is accessed through five pins

TCK: test clock

TMS: test mode select

TDI: test data in

TDO: test data out

TRST*: test reset (optional)

Chips with internal scan chains can access the chains through boundary scan for unified test strategy.

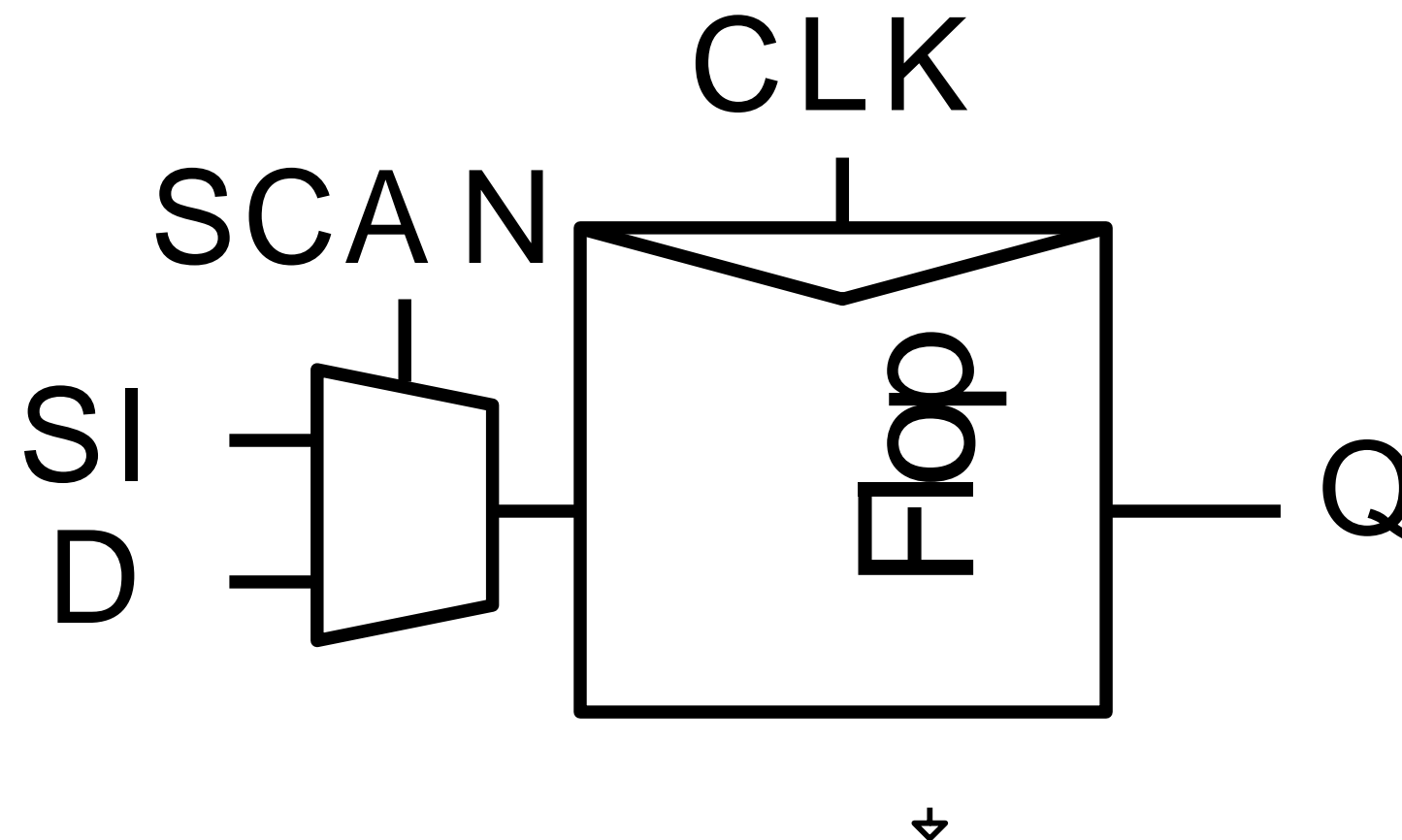


SIMULATE



Think about testing from the beginning
Simulate as you go
Plan for test after fabrication

“If you don’t test it, it won’t work! (Guaranteed)”





ASSESSMENT



WRITE THE BOUNDARY SCAN PIN NAMES
& FILL UP THE BLANK IN PRSG

TABLE

TCK:

TMS:

TDI:

TDO:

TRST*:

Step	Q
0	111
1	-----
2	101
3	-----
4	100
5	-----
6	011
7	-----





SUMMARY & THANK YOU