

SNS COLLEGE OF TECHNOLOGY

Coimbatore-35 An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB231 – DIGITAL ELECTRONICS

II YEAR/ III SEMESTER

NAND-NOR Implementation /19ECB231/ DIGITAL ELECTRONICS/K.SURIYA, AP/ECE/SNSCT

UNIT 1 – MINIMIZATION TECHNIQUES AND LOGIC GATES

TOPIC – NAND-NOR IMPLEMENTATION

26-Oct-2







NAND and NOR implementation

> Any Boolean function can be created using AND OR and NOT gates.

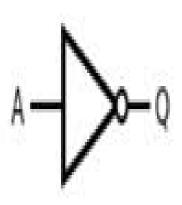
>AND, OR and NOT gates can be implemented using NAND and NOR gates.



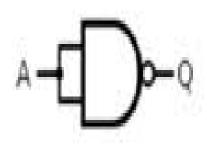


NAND implementation - Implementation of **NOT and AND using NAND gate**

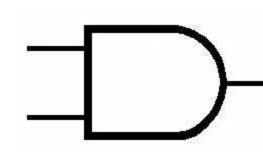
A NAND gate with single input acts like a NOT gate. \triangleright As a NAND gate is the invert of AND so by putting an inverter on the output of NAND we can have AND gate.



NOT gate



NAND construction of NOT ga

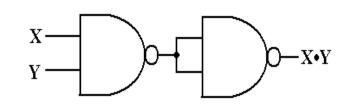


AND Gate

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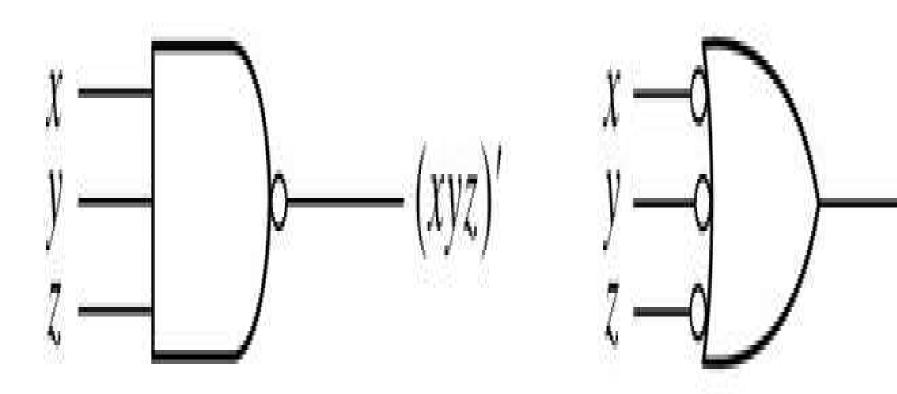




NAND Construction of ANDG ate



Symbolic Equivalence of NAND Gate



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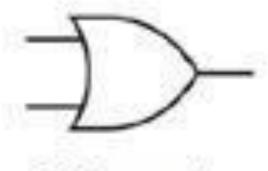
-x'+y'+z'=(xyz)'

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NOR implementation - Implementation of OR gate using NOR gate

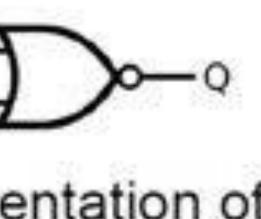
 \succ As NOR is the invert of OR gate so by putting an inverter in the output of NOR we get OR gate



OR gate

NOR implementation of OR gate

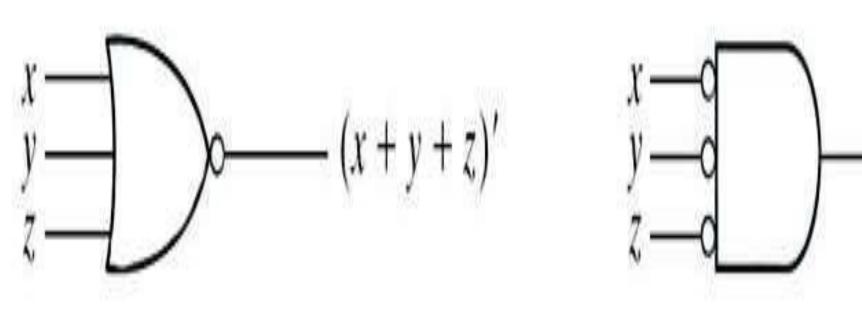






Graphical equivalence of NOR gate

> By De Morgan's Law we can describe NOR gate graphically by the following symbols







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to DR moyan's theorem)

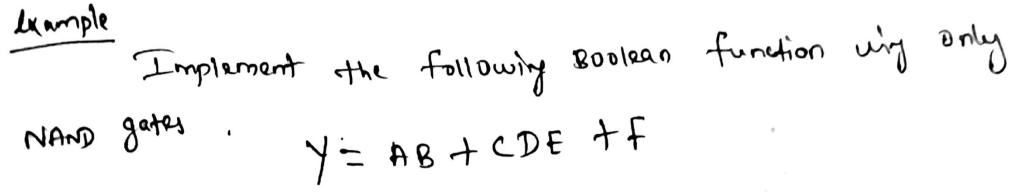
+6+5

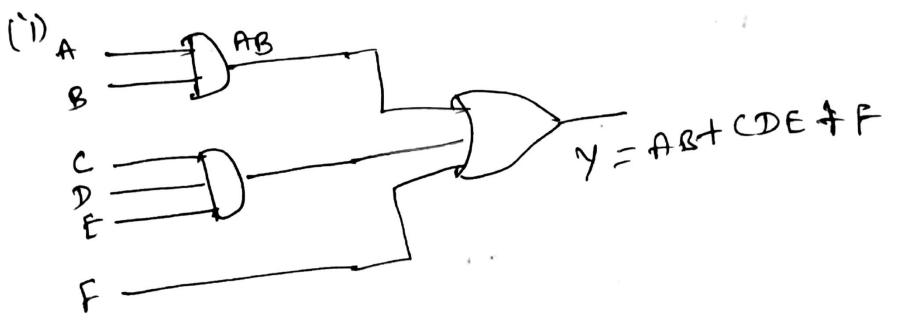
d convert of in the

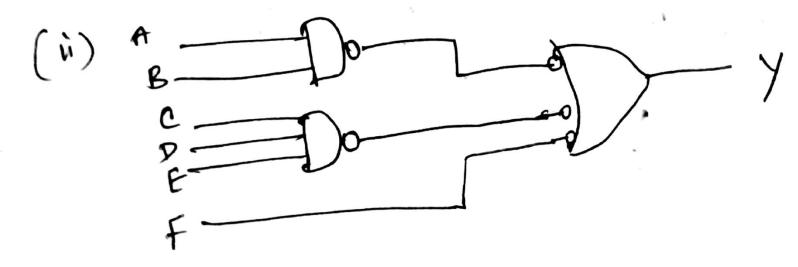
eng DR gate NAND invertag

NAND gates







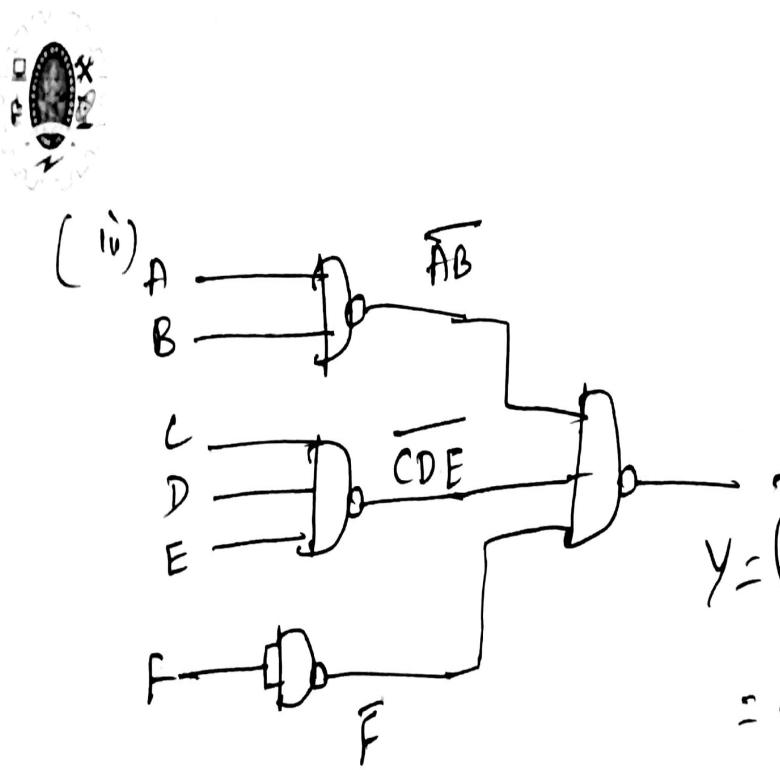


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 $Y = (\overline{AB})(\overline{CDE})(\overline{F})$

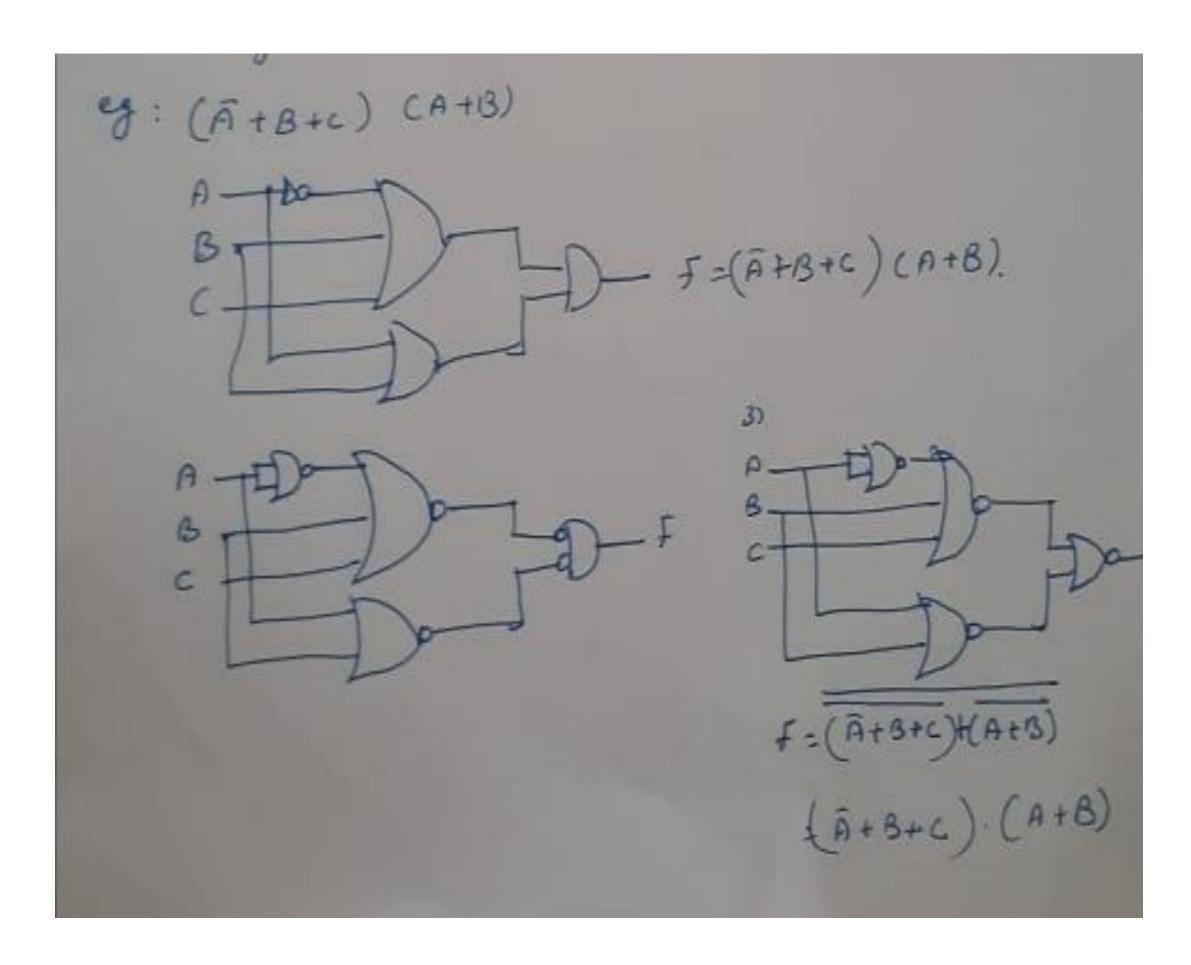
= AB+ (DE+F



NOR-NOR Implementation! -NOR = Bubbled AND $-\frac{1}{A+B+C} = \frac{A-\Phi}{C} + \frac{A}{B} + \frac{A}{C} + \frac{A}{C}$ (i) expression convert it into por fam procedure (ii) draw AND-OR-NOT redization (iii) Replace every OR gete by NOR, AND by a bubbled AND gate and inverter by a NOR invertey (i) Finally, draw the final circuit by only the NOR gates







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THANK YOU

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