SNS COLLEGE OF TECHNOLOGY

Coimbatore-35

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF COMPUTER SCIENCE ENGINEERING

19ECB231 – DIGITAL ELECTRONICS

II YEAR/ III SEMESTER

UNIT 1 – **MINIMIZATION TECHNIQUES AND LOGIC GATES**

TOPIC –IMPLEMENTATION OF LOGIC FUNCTIONS USING GATES

Two Level Implementation of Boolean function

- Two level logic means that the logic design uses maximum two logic gates between input and output. This does not mean that the whole design will contain only two logic gates but the single path from input to output may contain no more than two logic gates.
- For two-level logic implementation, we consider four logic gates i.e. AND gate, OR gate, NAND gate, and NOR gate. If we use one of these four gates at first level and one at the second level then we get a total of 16 combinations of two-level logic.
- Each two-level combination implements different logic functions, There are two main types in these 16 combinations.
- **Degenerate Form**
- **Non-Degenerate Form**

Degenerate Form

- The two-level combination that degenerates into a single logic function as known as degenerate form.
- There are 8 degenerate forms in those 16 combinations.

AND-AND Combination

OR-OR Combination

AND-NAND Combination

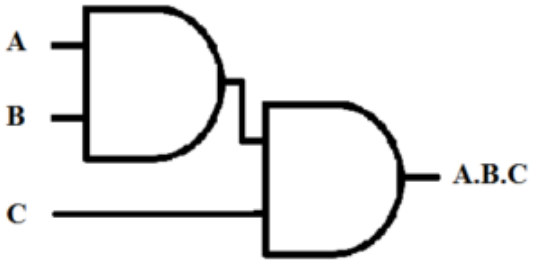
OR-NOR Combination

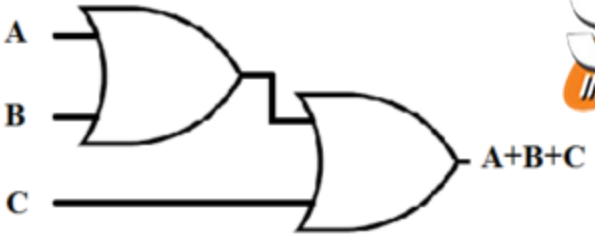
NAND-NOR Combination

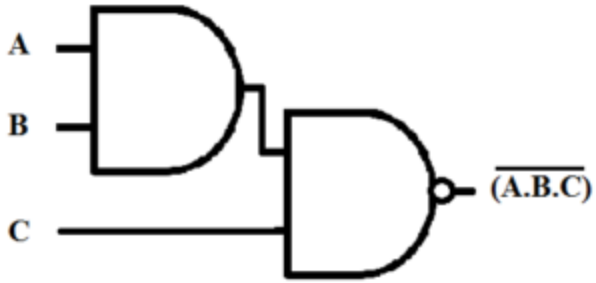
NOR-NAND Combination

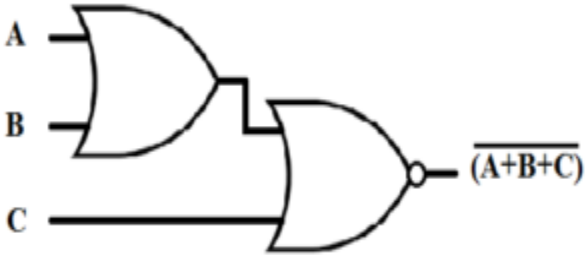
NAND-OR Combination

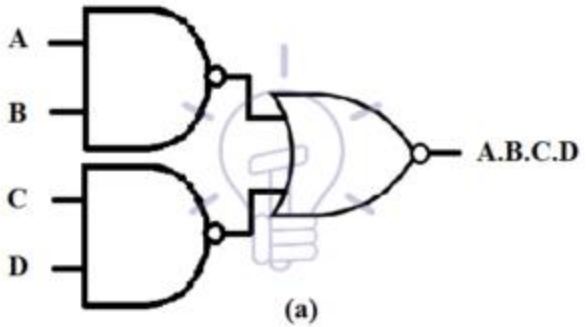
NOR-AND Combination





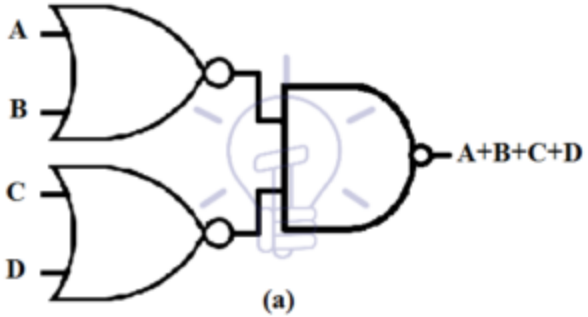






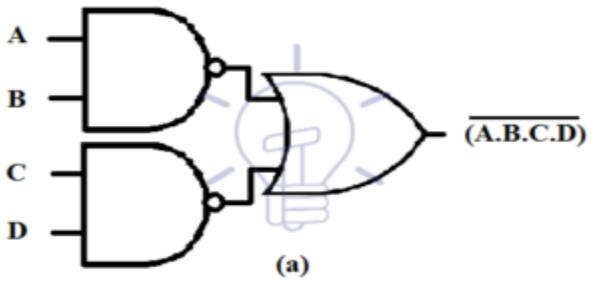
Schematic of NAND-NOR Combination

((A.B)'+(C.D)')' = (A.B.C.D)



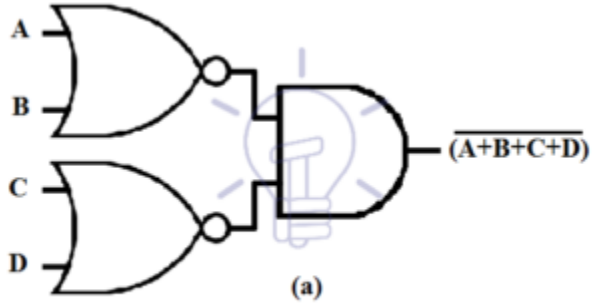
Schematic of NOR-NAND Combination

((A + B)'(C + D)')' = (A + B + C + D)



Schematic of NAND-OR Combination

((A . B)'+(A . B)')=(A . B . C . D)'



Schematic of NOR-AND Combination

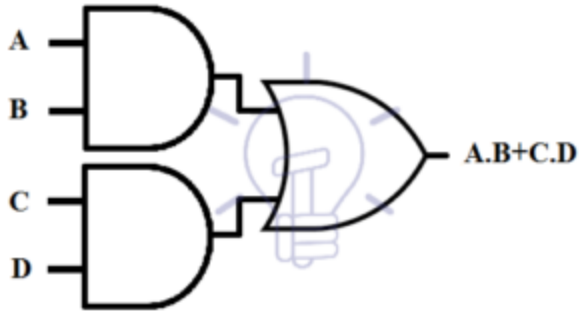
(A + B)'. (C + D)'=(A+B+C+ D)'

Non-Degenerate Form

- Those combinations of Two-level logic, which implements Sum of Product form or Product of sum form are Non-degenerate forms.

1. AND-OR

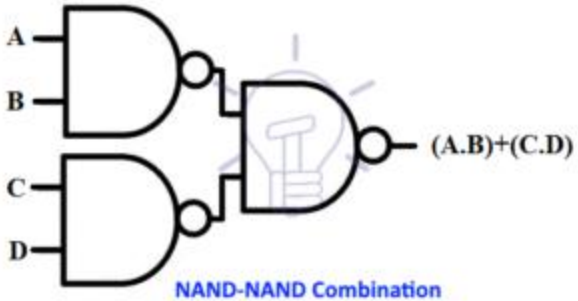
A . B + C . D



AND-OR Combination

2. **NAND-NAND**

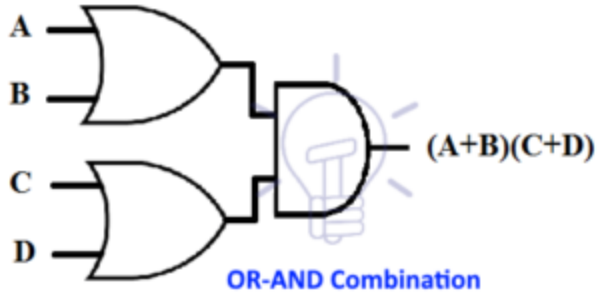
((A . B)’ (C . D)’)’=(A . B)+(C . D)



NAND-NAND Combination

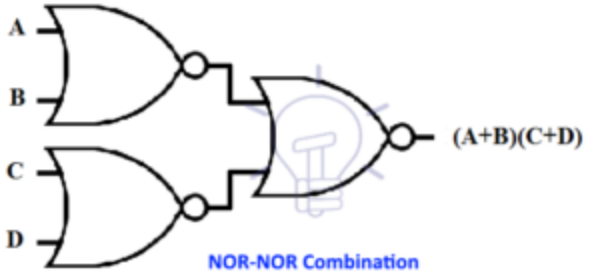
3. OR-AND

(A + B) (C + D)



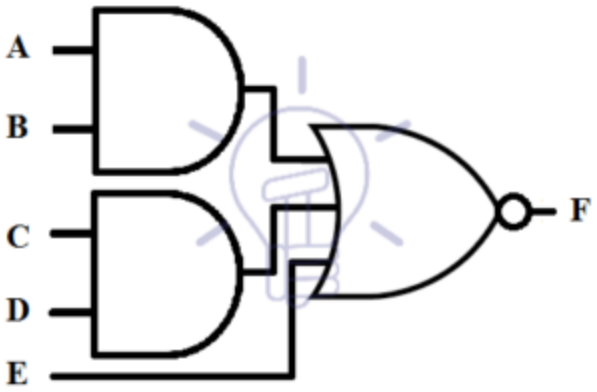
4. NOR-NOR

((A + B)'+(C+D)')' = (A + B) (C + D)



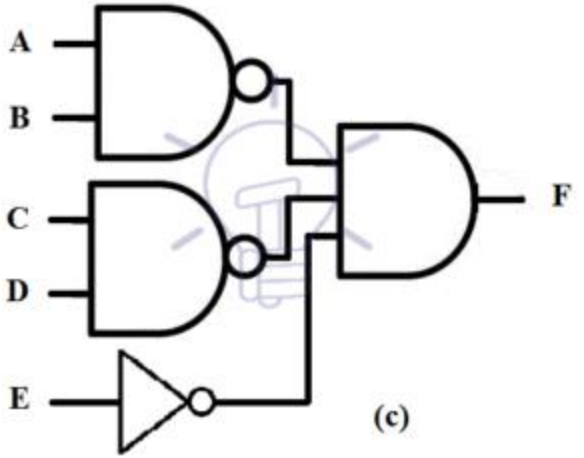
5. AND-NOR

F = (AB + C D + E)'



6. NAND-AND

F = (AB + C D + E)'

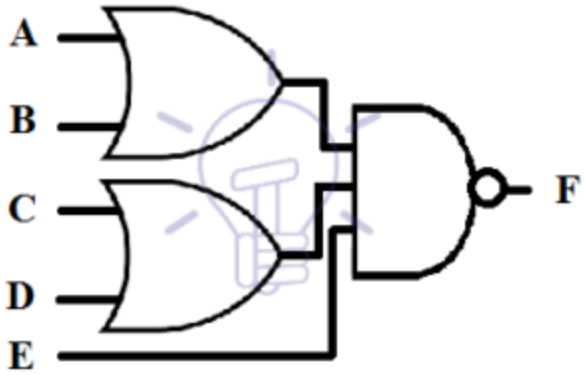


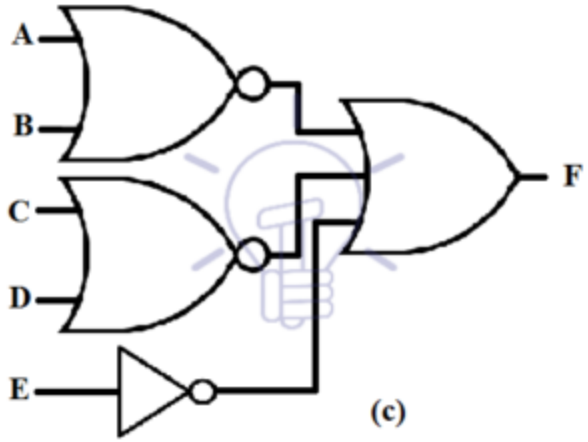
7. **OR-NAND**

[(A+B) (C + D) E]'

8. NOR-OR

(A + B)' + (C + D)' = [(A + B) (C+D]'





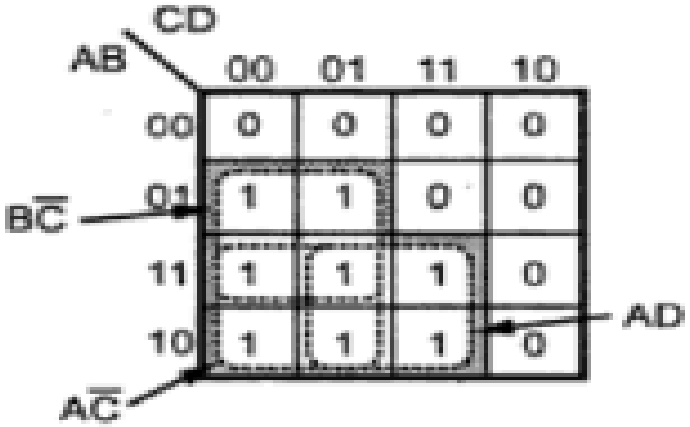
Two Level Implementation of Boolean function

- Minimize the following function using K-map

$$Y = \sum m(4, 5, 8, 9, 11, 12, 13, 15)$$

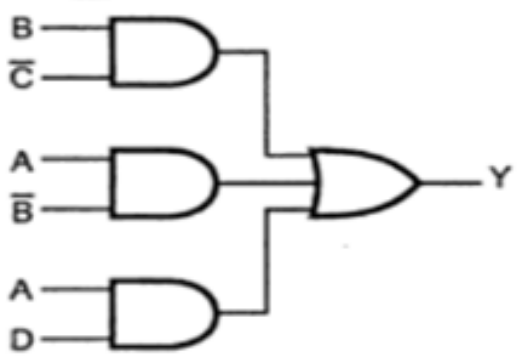
Solution:

K-Map Simplification:



Expression: Y= BC' + AB' + AD

Logic Diagram:



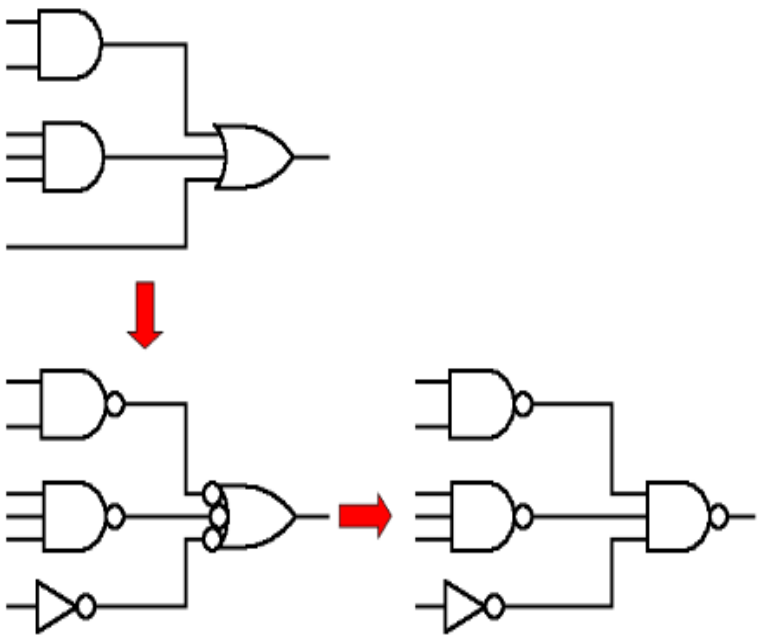
Multi Level Implementation of Boolean function

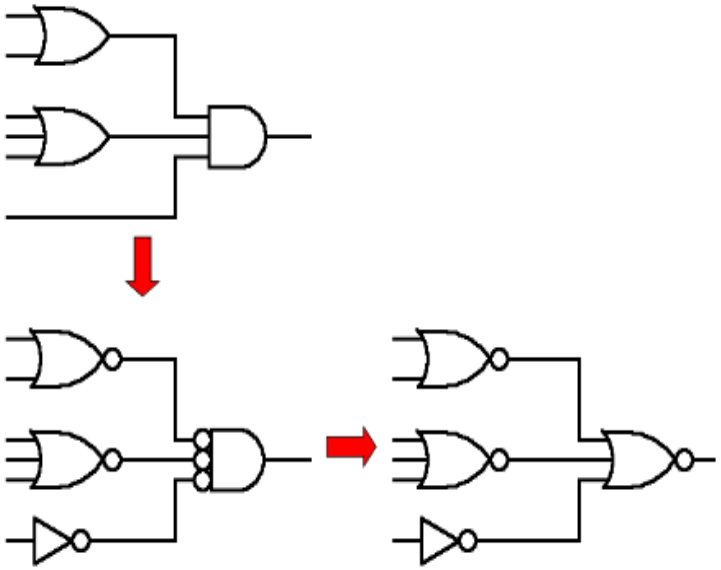
- Multilevel NAND & NOR circuits - Two-level circuits consisting of AND and OR gates can easily be converted to networks that can be realized only NAND and NOR gates
- A two-level AND-OR (SOP) circuit can be realized (directly) as a two-level NAND-NAND circuit
- A two-level OR-AND (POS) circuit can be realized (directly) as a two-level NOR-NOR circuit•
- The same approach can be used for multilevel networks

AND-OR to NAND-NAND example

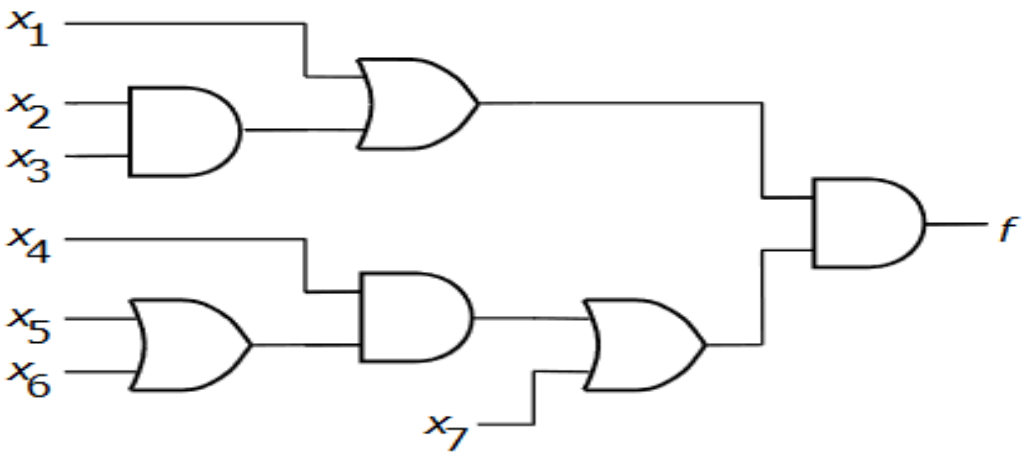
example

OR-AND to NOR-NOR



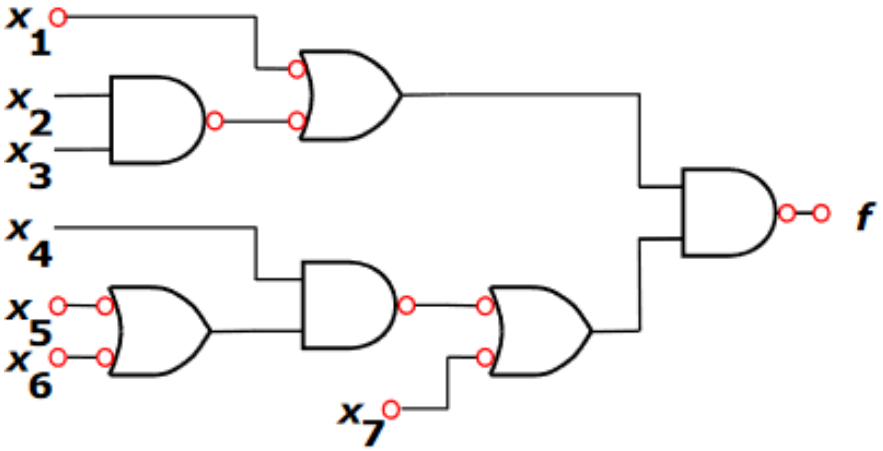


Multilevel example



Circuit with AND and OR gates

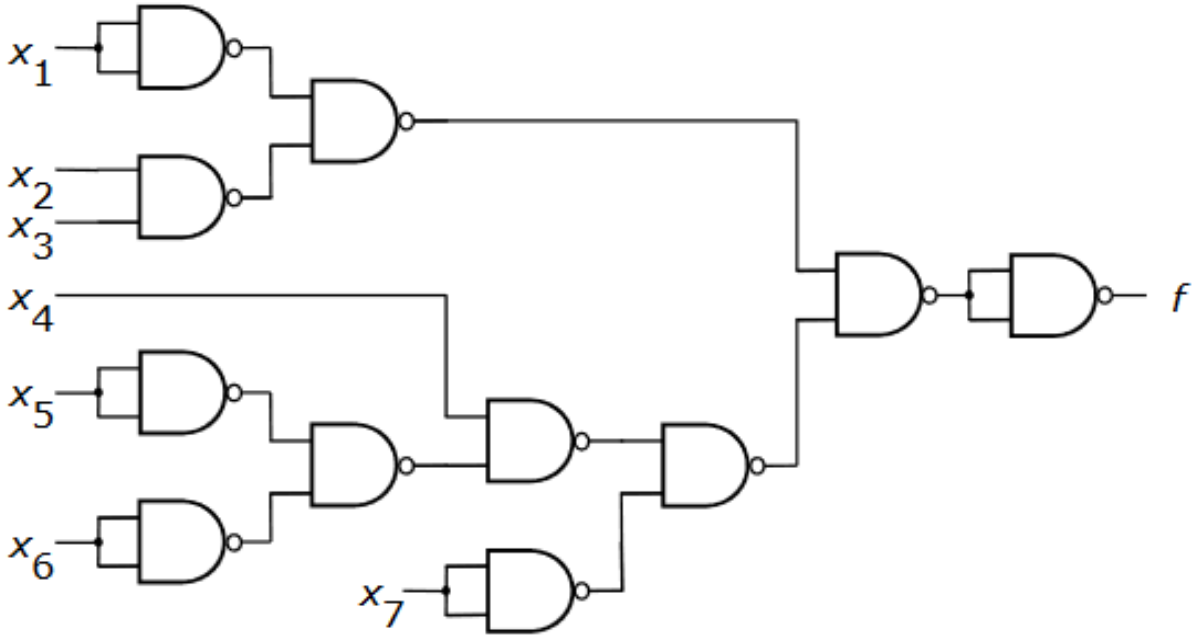
Multilevel example (NAND)



Inversions needed to convert to NANDs

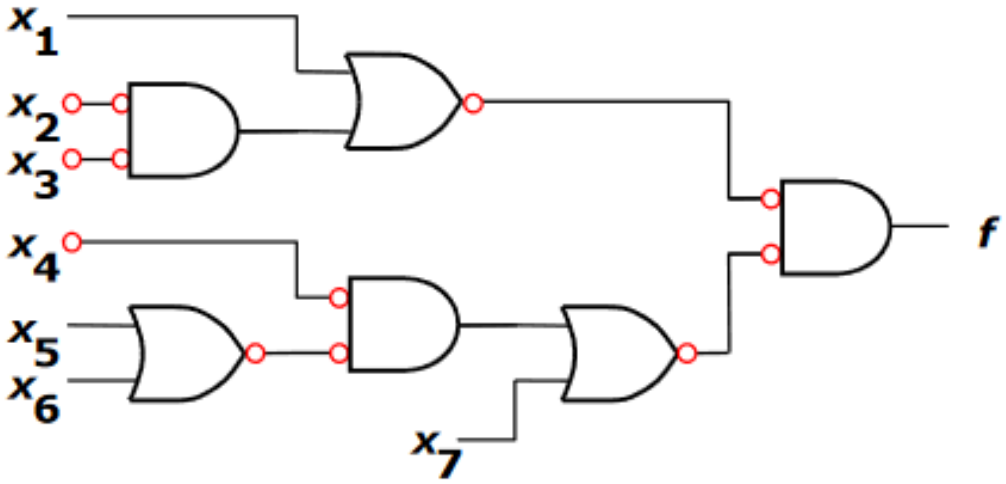
Note the inversion bubbles added to the output of every AND gate and to the input of every OR gate. Also, the inversion bubbles are always placed in pairs.

Multilevel example (NAND)



Conversion to a NAND-gate circuit

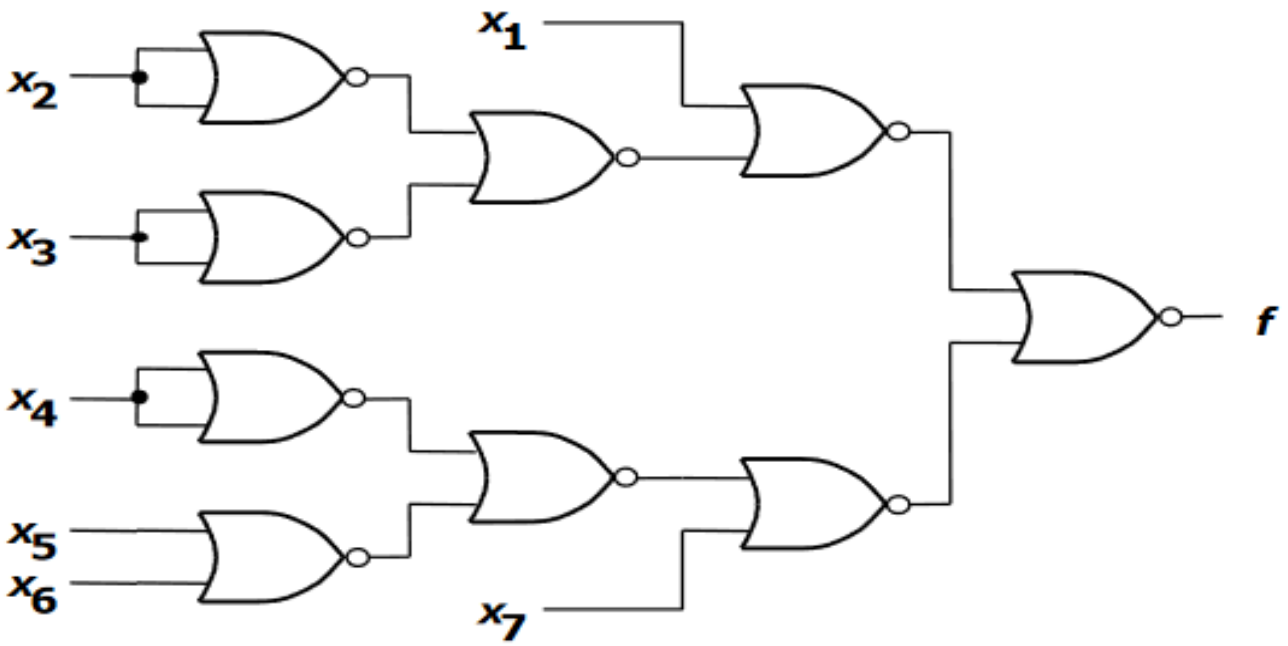
Multilevel example (NOR)



Inversions needed to convert to NORs

Note the inversion bubbles added to the output of every OR gate and to the input of every AND gate. Also, the inversion bubbles are always placed in pairs.

Multilevel example (NOR)



Conversion to a NOR-gate circuit

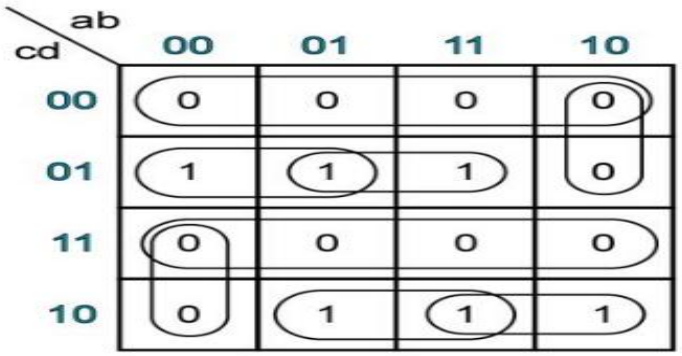
Multi Level Implementation of Boolean Function

Minimize the following function using K-map

$F(A, B, C, D) = \sum m (1,5,6,10,13,14)$

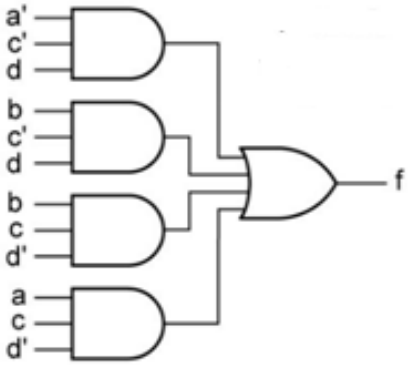
Solution:

K Map Simplification:



Expression: F= A'C'D + BC'D + BCD' + ACD'

Logic Diagram:



THANK YOU