



**SNS COLLEGE OF TECHNOLOGY**  
**Coimbatore-35**  
**An Autonomous Institution**



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**DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING**

**19ECB231 – DIGITAL ELECTRONICS**

II YEAR/ III SEMESTER

UNIT 2 – COMBINATIONAL CIRCUITS

TOPIC - PARALLEL BINARY ADDER/SUBTRACTOR



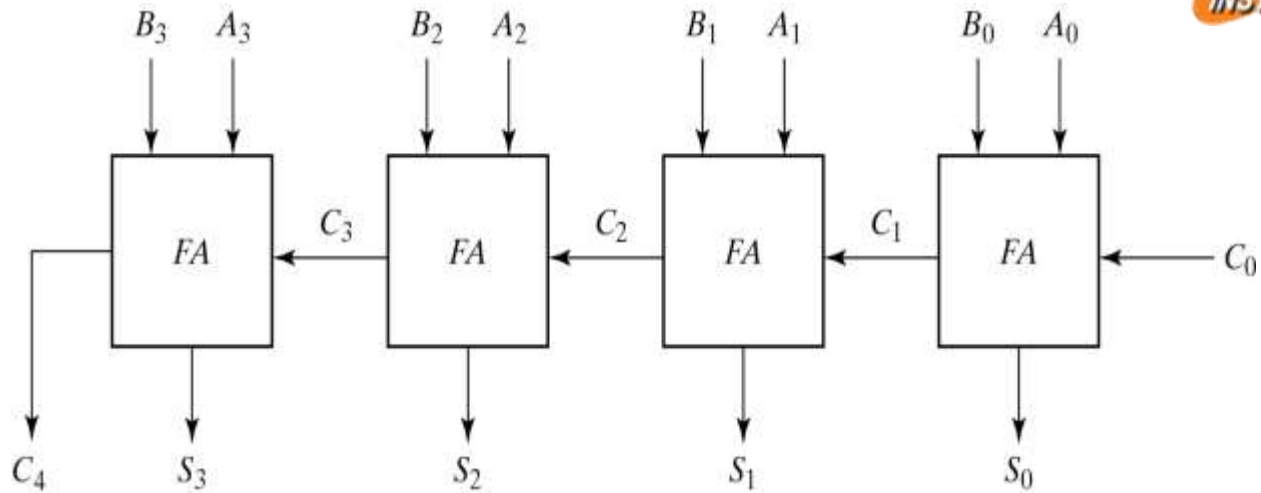
# BINARY ADDER



- A “ripple carry adder” is simply “n”, 1-bit full adders cascaded together with each full adder representing a single weighted column in a long binary addition.
- It is called a ripple carry adder because the carry signals produce a “ripple” effect through the binary adder from right to left, (LSB to MSB).
- For example, suppose we want to “add” together two 4-bit numbers, the two outputs of the first full adder will provide the first place digit sum (S) of the addition plus a carry-out bit that acts as the carry-in digit of the next binary adder.



# 4-bit Ripple Carry Adder



| <b>Subscript <math>i</math>:</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |           |
|----------------------------------|----------|----------|----------|----------|-----------|
| Input carry                      | 0        | 1        | 1        | 0        | $C_i$     |
| Augend                           | 1        | 0        | 1        | 1        | $A_i$     |
| Addend                           | 0        | 0        | 1        | 1        | $B_i$     |
| Sum                              | 1        | 1        | 1        | 0        | $S_i$     |
| Output carry                     | 0        | 0        | 1        | 1        | $C_{i+1}$ |



## Disadvantage of Ripple Carry Adder

- When the inputs A and B change, the sum at its output will not be valid until any carry-input has “rippled” through every full adder in the chain because the MSB (most significant bit) of the sum has to wait for any changes from the carry input of the LSB (less significant bit).
- Thus there will be a finite delay before the output of the adder responds to any change in its inputs resulting in a accumulated delay.
- This unwanted delay time is called **Propagation delay**.



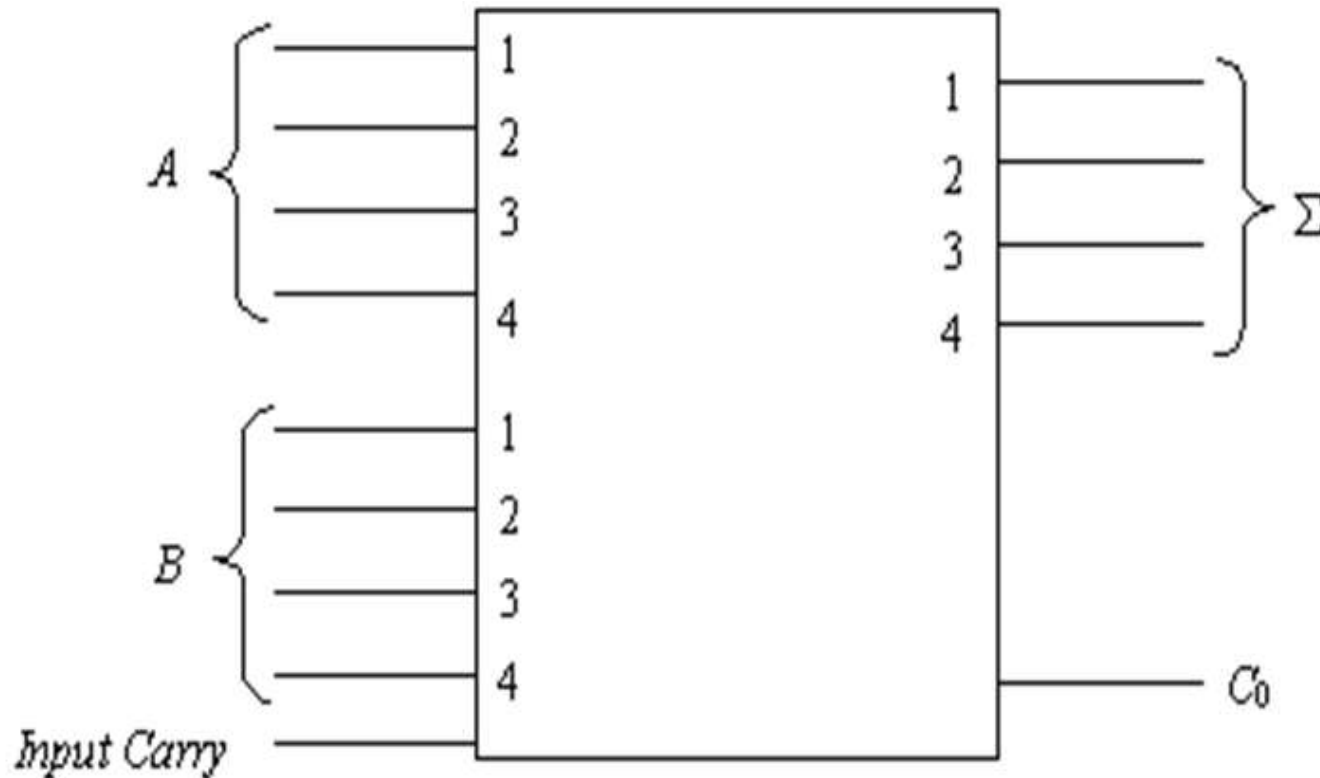
- Consider the above figure, in which the sum  $S_3$  is produced by the corresponding full adder as soon as the input signals are applied to it.
- But the carry input  $C_3$  is not available on its final steady state value until carry  $C_2$  is available at its steady state value. Similarly  $C_2$  depends on  $C_1$  and  $C_0$ .
- Therefore, carry must propagate to all the stages in order that output  $S_3$  and carry  $C_2$  settle their final steady-state value.
- The propagation time is equal to the propagation delay of the typical gate times the number of gate levels in the circuit.



- Another problem called “**overflow**” occurs when an n-bit adder adds two parallel numbers together whose sum is greater than or equal to  $2^n$
- One solution is to generate the carry-input signals directly from the A and B inputs rather than using the ripple arrangement
- Another type of binary adder circuit called a Carry Look Ahead Binary Adder was introduced where the speed of the parallel adder can be greatly improved using carry-look ahead logic.

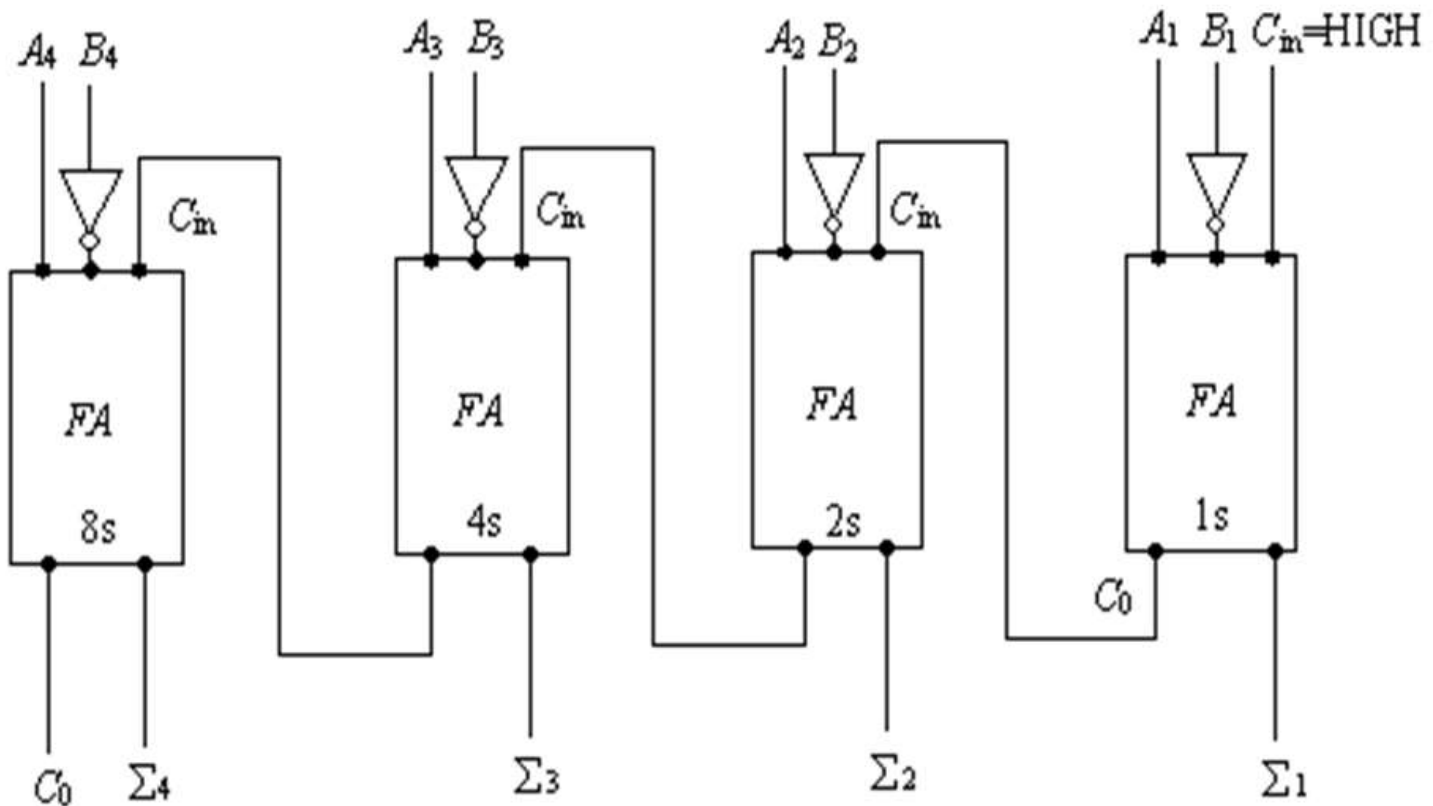


## Logic Symbol Of Four Bit Parallel Adder





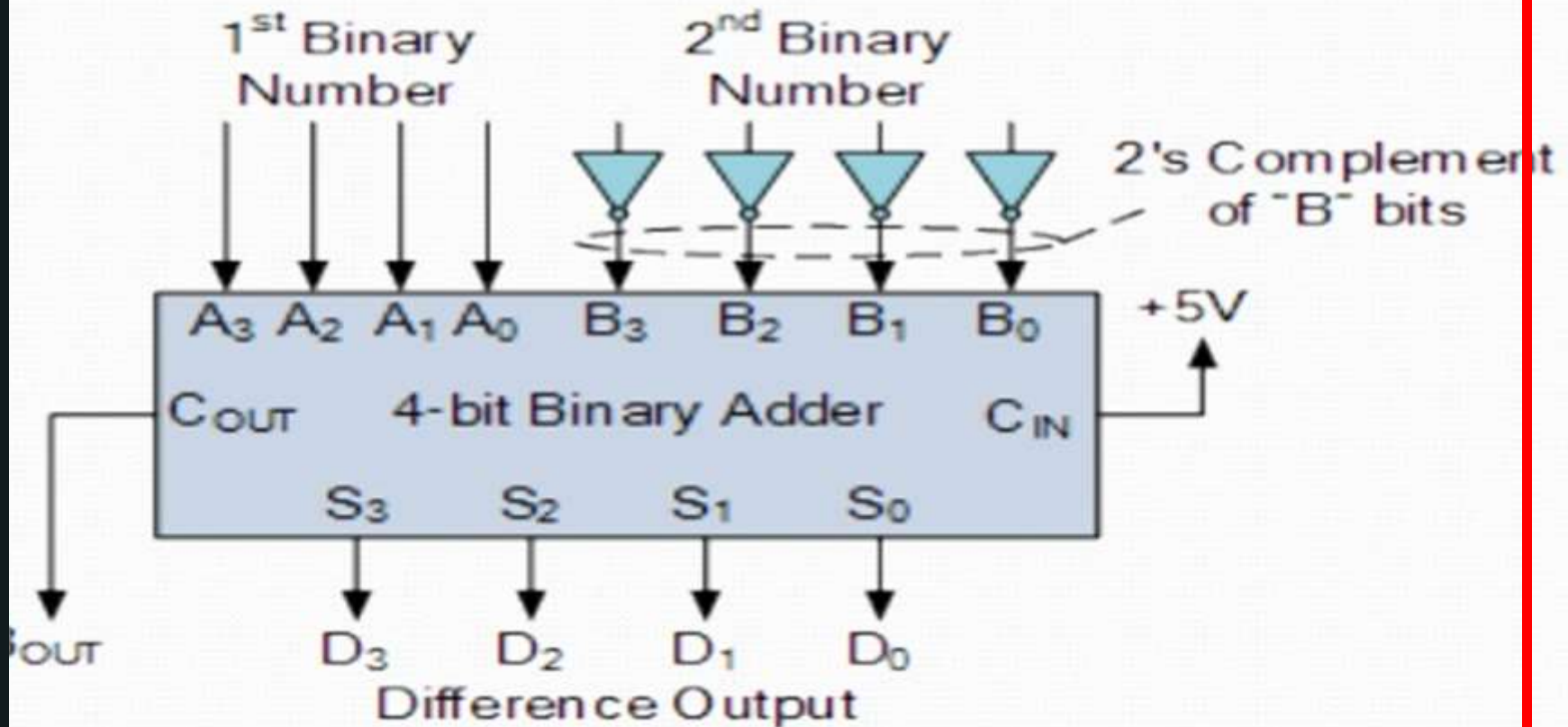
# Four Bit Parallel Subtractor using Full Adders







When 1 is added to 1s complement of B, by making  $c_{in}=1$ . Thus we obtain the 2s complement of B.





# BINARY ADDER/SUBTRACTOR

- A **Binary Adder-Subtractor** is one which is capable of both addition and subtraction of binary numbers in one circuit itself.
- The operation being performed depends upon the binary value the control signal holds.
- The addition and subtraction operations can be combined into one circuit with one common binary adder by including an exclusive-OR gate with each full-adder



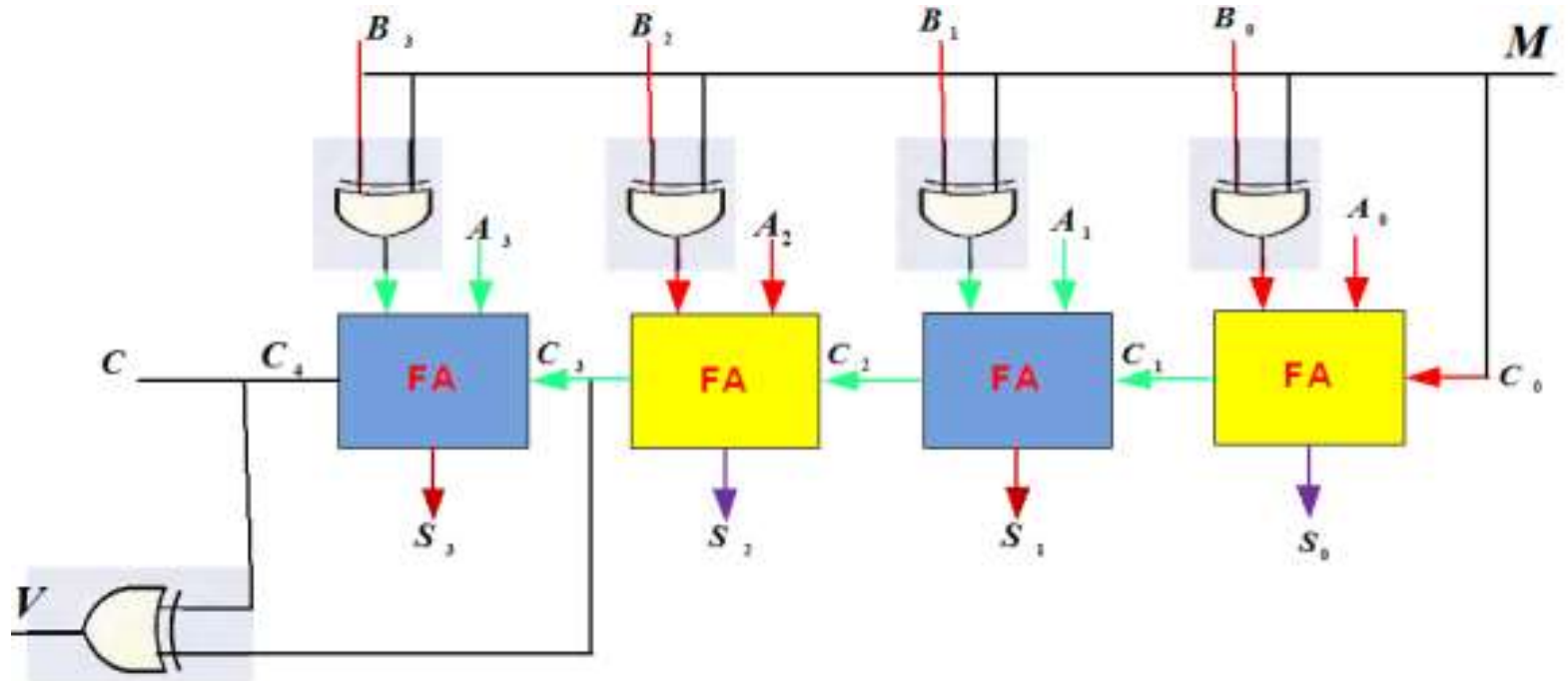
# BINARY ADDER/SUBTRACTOR



- Consider two 4-bit binary numbers A and B as inputs to the Digital Circuit for the operation with digits
- $A_0 A_1 A_2 A_3$  for A  $B_0 B_1 B_2 B_3$  for B
- The circuit consists of 4 full adders since we are performing operation on 4-bit numbers.
- There is a control line M that holds a binary value of either 0 or 1 which determines that the operation being carried out is addition or subtraction.



# BINARY ADDER/SUBTRACTOR





## Explanation:



The mode input  $M$  controls the operation as the following:

- $(M = 0 \rightarrow$  adder.
- $M = 1 \rightarrow$  subtractor.
- Each **XOR** gate receives  $M$  signal and  $B$ 
  - When  $M = 0$  then  $B \oplus 0 = B$  and the carry =  $0$ , then the circuit performs the operation  $A + B$ .
  - When  $M = 1$  then  $B \oplus 1 = \bar{B}$  and the carry =  $1$ , then the circuit performs the operation  $A - B$ .
- The **exclusive-OR** with output  $V$  is for detecting an overflow.



Example:

Consider two 3 bit numbers  $A=010$  and  $B=011$  and input them in the full adder with both values of control lines.

### Binary Addition:

For  $M=0$ :

$B_0(\text{exor})M=B_0$  and  $C_0=M=0$

Thus from first full adder =  $A_0+B_0 = 0+1 = 1$ ,  $S_0=1$   $C_1=0$  Similarly,  $S_1=0$  with  $C_2=1$

$S_2=1$  and  $C_2=0$

Thus,  $A = 010 = 2$   $B = 011 = 3$   $\text{Sum} = 0101 = 5$



## Binary Subtraction:

For  $K=1$

$B_0(\text{exor})K=B_0'$  and  $C_0=k=1$

Thus  $S_0=1$  and  $C_1=0$

Similarly  $S_1=1$  and  $C_2=0$

$S_3=1$  and  $c_3=1$

Thus,  $A = 010 = 2$   $B = 011 = 3$

Sum(Difference) =  $1111 = -1$



**THANK YOU**