SNS COLLEGE OF TECHNOLOGY

Coimbatore-35

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB231 – DIGITAL ELECTRONICS

II YEAR/ III SEMESTER

UNIT 2 – COMBINATIONAL CIRCUITS

TOPIC - CARRY LOOK AHEAD ADDER

Ripple Carry Adder

- n-bit Ripple Carry Adder
  - Composed of n 1-bit Full Adders
  - Carries ripple from LSB stage to MSB stage
    - Delay ~ (n)*(delay of single FA stage)
    - Area required is linear in n
- 4-bit Ripple Carry Adder
  - Composed of 4 1-bit Full Adders

The Ripple Carry Adder is slow!

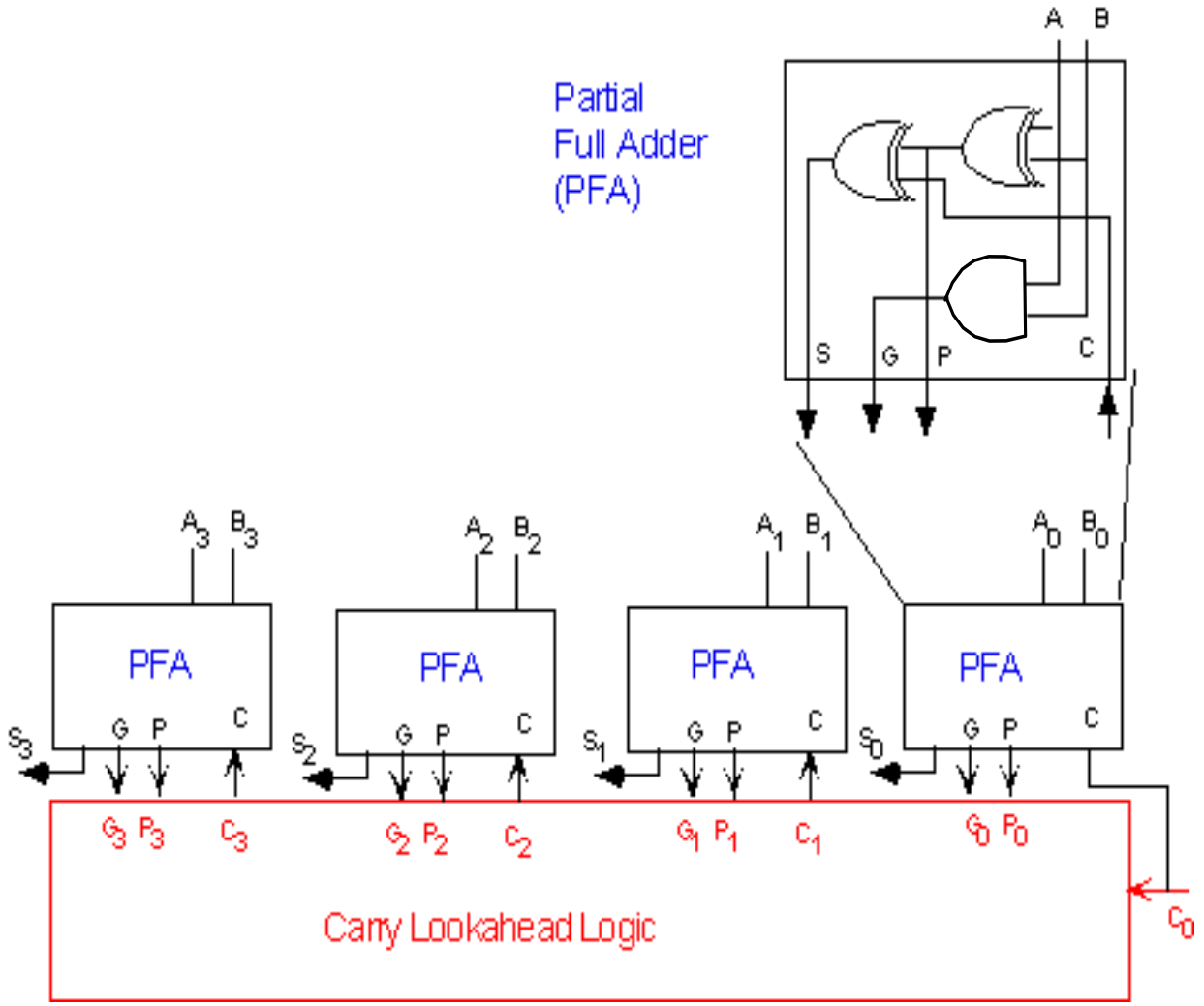
Why?

How can the speed of the adder be increased?

- Carry Lookahead Adder

Generate signal: g_i
Propagate signal: p_i

Carry Look-Ahead Adder Design



$C_{i+1} = G_i + P_i.C_i$

$G_i = A_i.B_i$

$P_i = (A_i \oplus B_i)$

Expressions

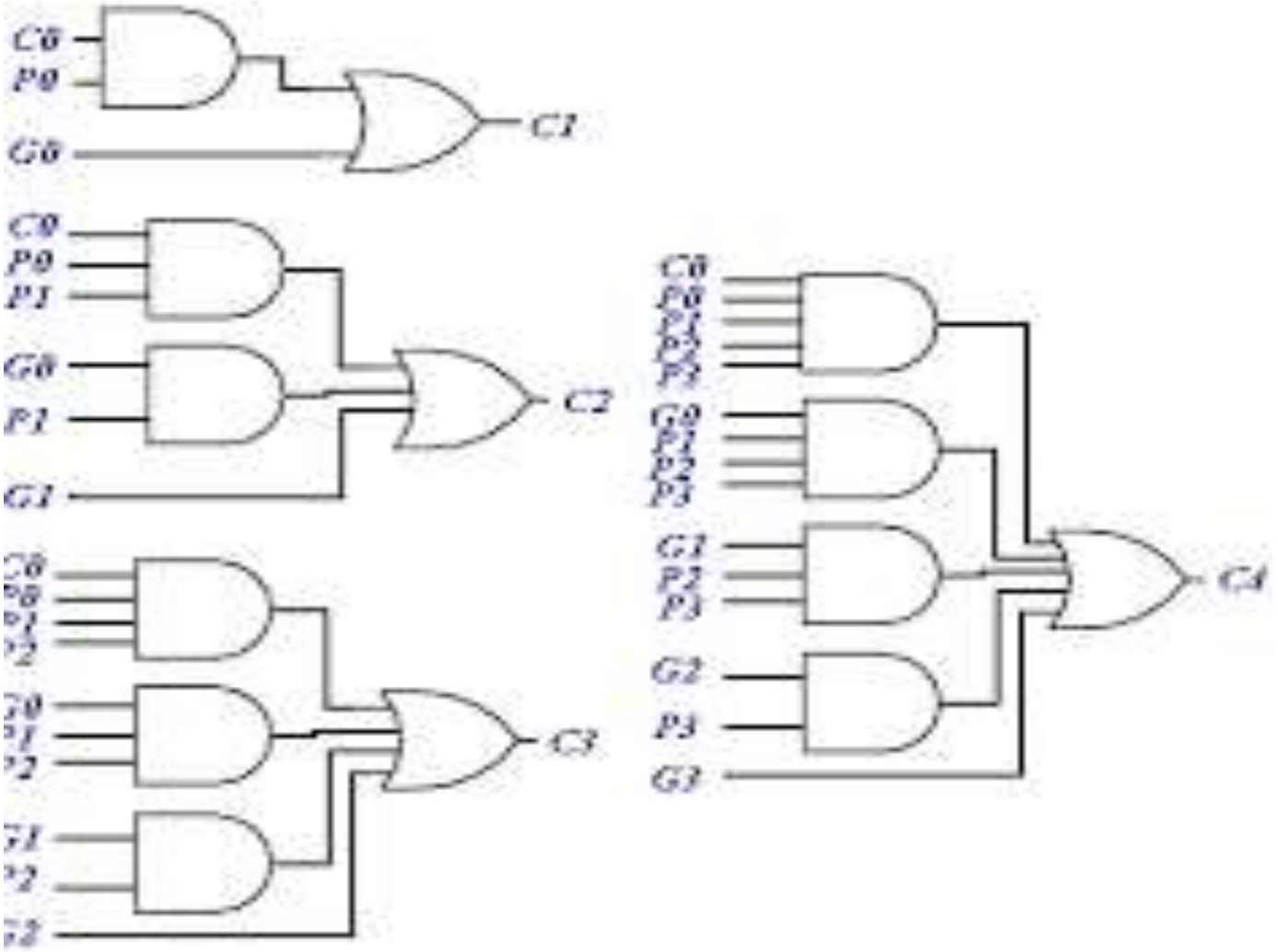
4-Bit Carry Look-Ahead Adder

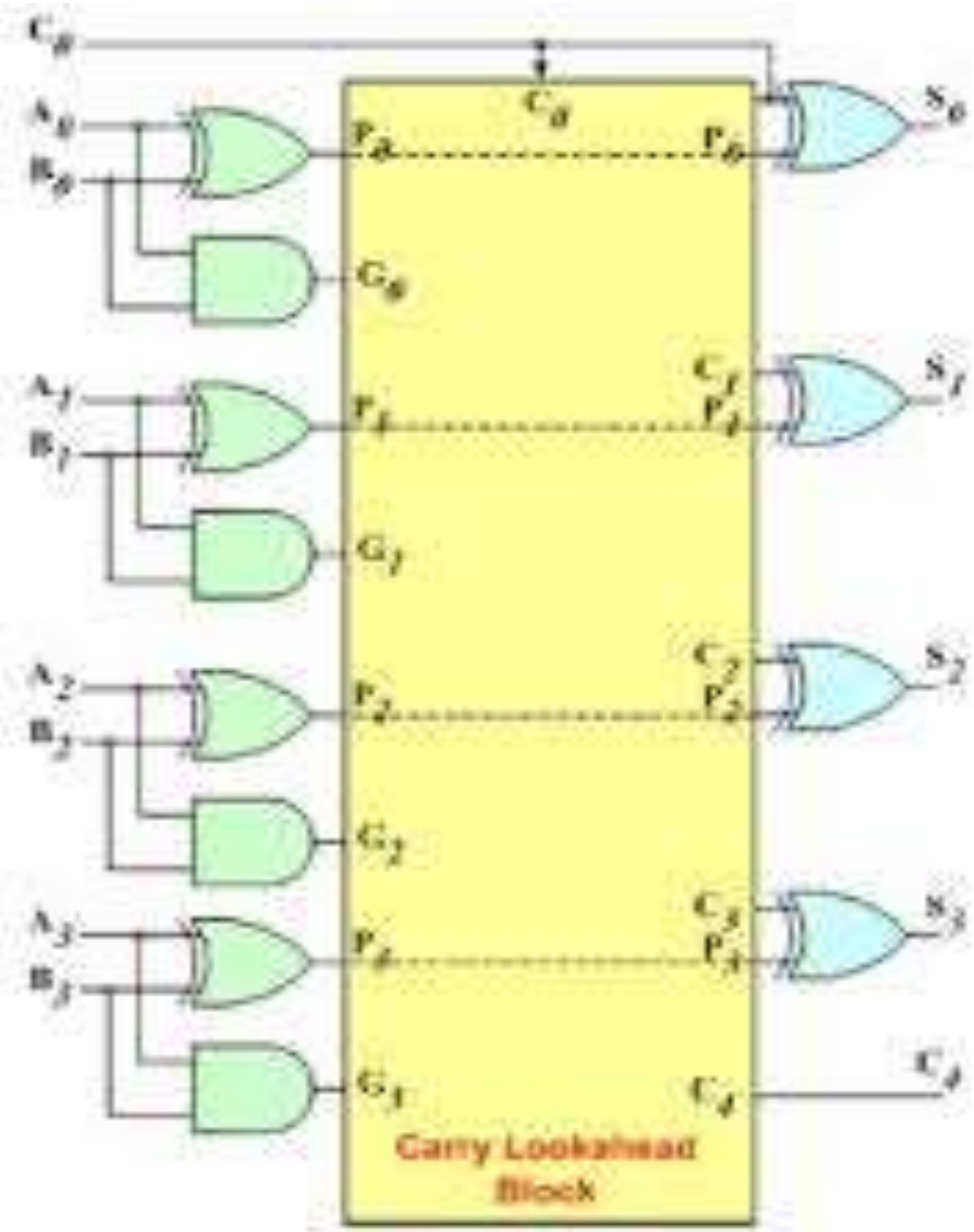
$$G_i = A_i B_i$$
$$P_i = A_i - B_i$$

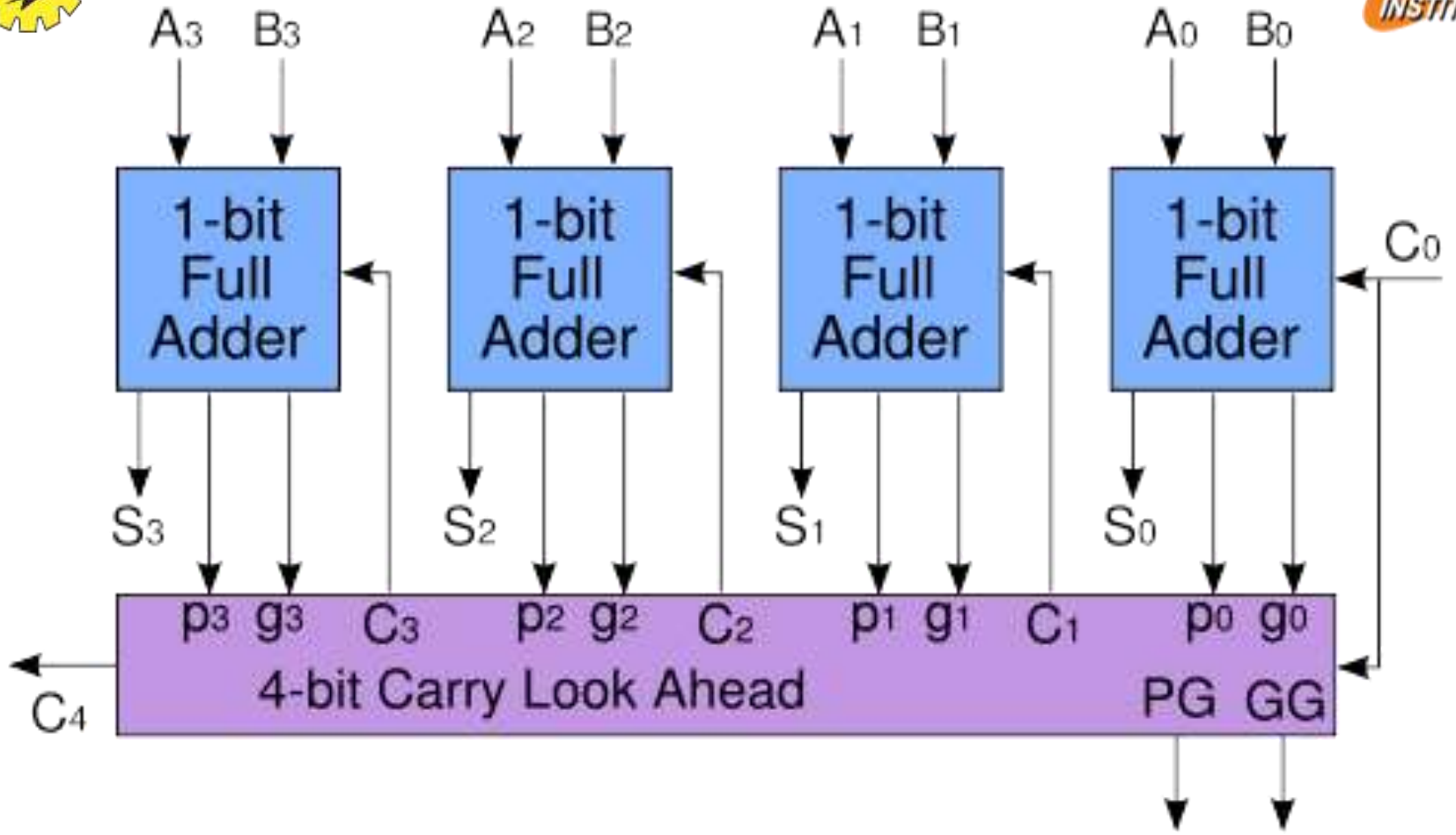
$$\Rightarrow C_i = G_i + P_i C_{i-1}$$

$$C_0 = G_0 + P_0 C_{-1} = G_0$$
$$C_1 = G_1 + P_1 C_0 = G_1 + P_1 G_0$$
$$C_2 = G_2 + P_2 C_1 = G_2 + P_2 (G_1 + P_1 C_0) = G_2 + P_2 G_1 + P_2 P_1 C_0$$
$$C_3 = G_3 + P_3 C_2 = G_3 + P_3 (G_2 + P_2 (G_1 + P_1 C_0))$$
$$= G_3 + P_3 (G_2 + P_2 G_1 + P_2 P_1 C_0)$$
$$= G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 C_0)$$

Logic circuit




Carry Lookahead
Block


A3 B3
A2 B2
A1 B1
A0 B0
1-bit Full Adder
1-bit Full Adder
1-bit Full Adder
1-bit Full Adder
C0
S3
S2
S1
S0
p3 g3 C3 p2 g2 C2 p1 g1 C1 p0 g0
4-bit Carry Look Ahead
PG GG
C4

Assessment Questions

1. Assume that the XOR gate has a propagation delay of 10ns and that the AND or OR gates have a propagation delay of 5ns.What is the total propagation delay time in the four bit adder.

2. Derive the two level Boolean expression for the output carry C4 for a look ahead carry generator.

THANK YOU