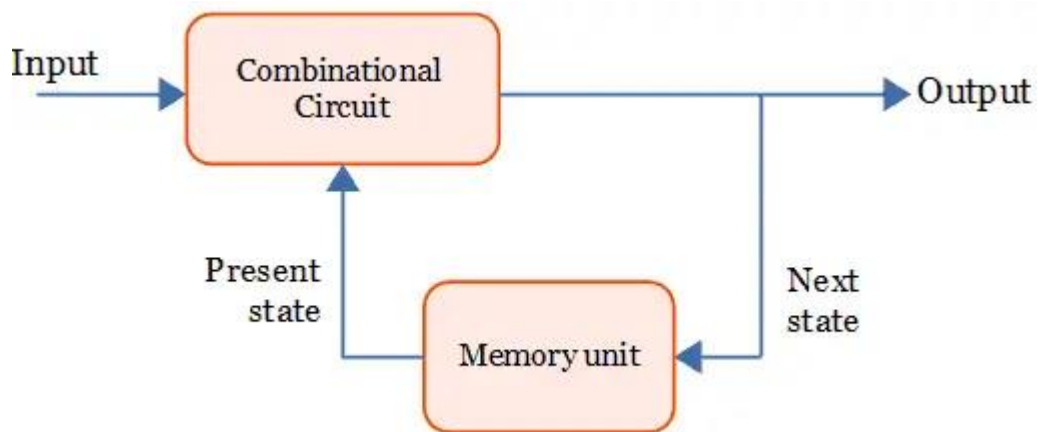# level triggering – edge triggering

The sequential circuit consists of a combinational logic, which gets the external input and the previous state output through the inbuilt memory unit as feedback. The memory unit may be a latch or a flip flop.

The present state and the external inputs determine the outputs and the next state of the sequential circuit. So, a sequential circuit works on a time sequence of external inputs, internal states and outputs.

How does a sequential circuit differ from a combinational circuit?

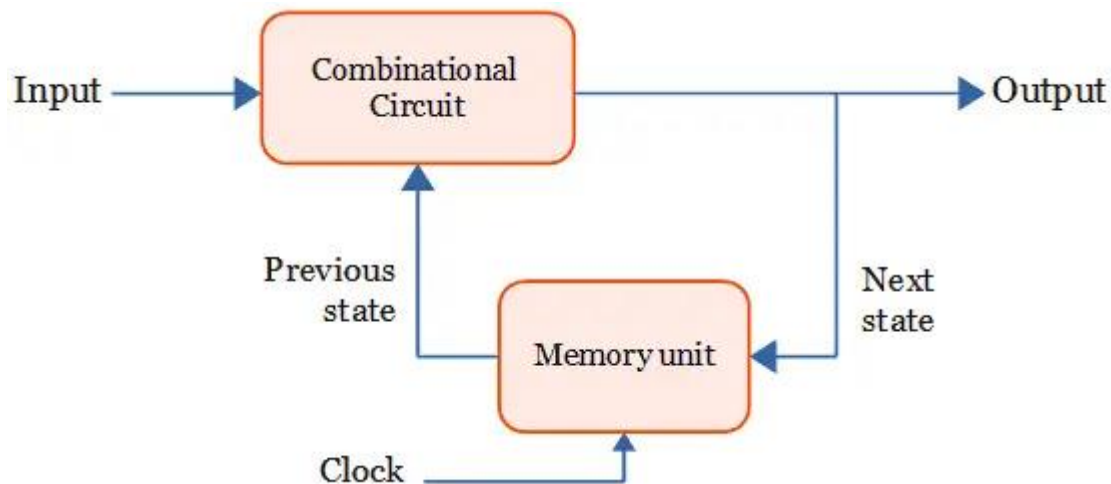| Combinational Circuit	Sequential Circuit
The output always depends on the combination of input variables.	The Output produced depends on both the present state and the next state variable.
A memory unit is not necessary.	Memory is necessary to store the next state variables.
The propagation delay is less due to the absence of memory units and so they are faster.	The speed is slower than combinational circuits.
Easy to design.	They are comparatively harder to design.

Types of Sequential Circuits

The sequential circuits are classified based on the clock pulses given to the memory units. There are two types as follows

1. Synchronous sequential circuit
2. Asynchronous sequential circuit.

Synchronous sequential circuit

In these circuits, change in input can affect the memory elements only upon the activation of the clock pulse. The memory units are clocked flip-flops.

The circuit will change its state for every clock pulse. Hence it is also called clocked sequential circuits.

The synchronous sequential circuits are represented by two models.

Moore model

In this sequential model, the output depends on the present state of the flip flops. An example of moore model circuit is shown in the below diagram. In this circuit, two JK flip flops are connected together.

The input is connected only to the first JK flip flop. The output is the multiplication of the next state output, but not of the input.

Mealy model

The output depends on the present state of the flip flops and the input. The circuit shown below is an example of Mealy circuit model. As you can see, the output is the product of the present state of flip flop and the input.

Asynchronous sequential circuit

The change in input signals can affect the memory element at any instant of time. The memory units do not have clock pulses. Instead, they have time delay elements.

What is a clock pulse?

A clock pulse is a continuously changing signal that oscillates between a high state and a low state. The common type of clock signal is a square type, which has 50% duty cycle with a fixed and constant frequency. A clock pulse is shown below.

While applying the clock pulse to the flip flop, it gets triggered by two ways, Level triggering and edge triggering.

Level triggering

In this, the flip flop is triggered only during the high-level or the low level of the clock pulse. In other words, the output changes its state, when active low or high level is maintained at the clock signal. Based on the level of triggering, it is of two types

- *Positive level triggering* – If the flip flop is triggered at the positive level of the clock pulse, then it is said to be a positive level triggering.
- *Negative level triggering* – If the flip flop is triggered at the negative level of the clock pulse, then it is said to be negative level triggering.

Flip flop is enabled only at High Level

(a) Positive Level triggering

Flip flop is enabled only at Low Level

(b) Negative Level triggering
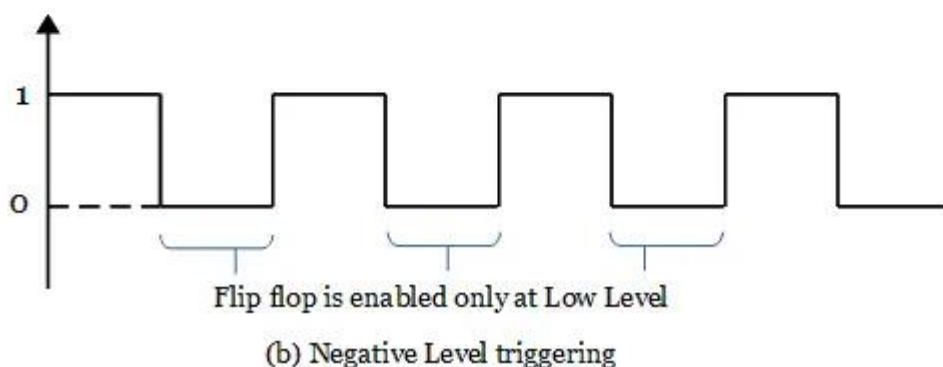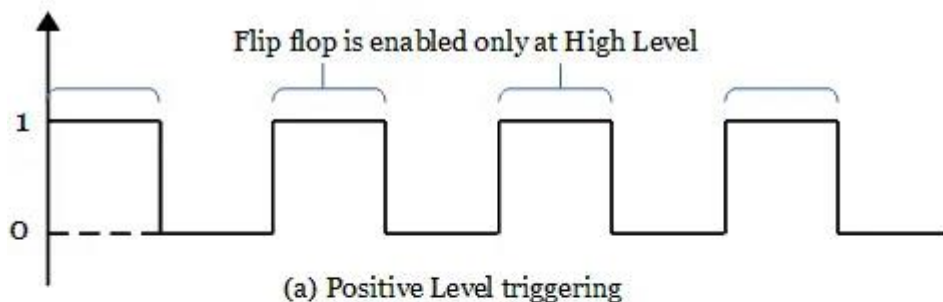
Edge triggering

In edge triggering, the flip flop changes its state during the positive edge or negative edge of the clock pulse. There are two types of edge triggering.

- *Positive edge triggering* – When the output responds to the change in the input only at the positive edge of the clock pulse, then the clock pulse is said to be a positive edge triggered.
- *Negative edge triggering* – When the output responds to the change in the input only at the negative edge of the clock pulse, then the clock pulse is said to be a negative edge triggered.

(a) Positive Edge triggering

(b) Negative Edge triggering