Reg.No: | | | | | | | |

SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)
Coimbatore – 641 035.

B.E / B.Tech – Internal Assessment Exam- I
Academic Year 2023-2024 (ODD)

Third Semester (Regulation R2019)

A

19ITT202 – Computer Organization and Architecture
(Common to CSE and IT)

TIME: 1.5 HOURS **MAXIMUM MARKS: 50**

ANSWER ALL QUESTIONS

PART A — (5 x 2 = 10 Marks)			
1.	Computer A has a clock cycle time of 250 ps and a CPI of 2.0 for some program, and computer B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program. Which computer is faster for this program and by how much?	CO1	Ana
2.	What is meant by straight line sequencing?	CO1	Und
3.	What is meant by Bus Structure in Computer Architecture?	CO1	Und
4.	Consider two 8 bit positive number +98 and +87 and perform	CO2	Ana
5.	Sketch the binary addition and subtraction logic Network	CO2	Und

PART B — (2 x 13 = 26 Marks and 1 x 14 = 14 Marks)

6.	(a)	(i) Formulate the CPU Performance equation and compose the various factors that affect performance	CO1	Ana	7
		(ii) Explain in detail about different instruction types and instruction sequencing with your own example.	CO1	Und	6
		(OR)			
	(b)	Define Addressing mode and explain the basic addressing modes with an example for each.	CO1	Und	13
7.	(a)	Explain in detail about addition and subtraction of signed number with diagram and example.	CO2	Und	13
		(OR)			
	(b)	Illustrate the concept of Carry Look ahead Adder with diagram.	CO2	Und	13

8.	(a)	Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively. C Code: f = g + A[B[4]- B[3]]; For the C statement above, what is the corresponding MIPS assembly code?	CO1	Ana	14
		(OR)			
8.	(b)	Show how to implement full adder by using two half adders and external logic gates.	CO1	Ana	14