

SNS COLLEGE OF TECHNOLOGY



Coimbatore-35
An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB231 – DIGITAL ELECTRONICS

II YEAR/ III SEMESTER

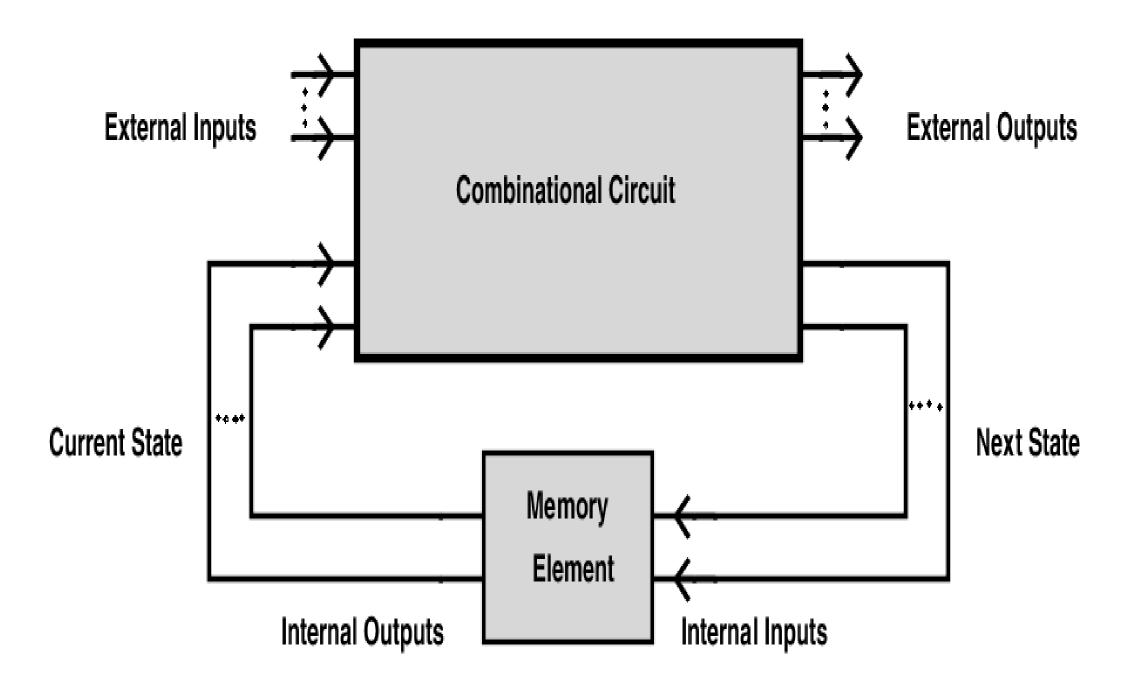
UNIT 3 – SEQUENTIAL CIRCUITS

TOPIC 1 - LATCHES



SEQUENTIAL CIRCUITS







SEQUENTIAL CIRCUITS



- This sequential circuit contains a set of inputs and outputs
- The outputs of sequential circuit depends not only on the combination of present inputs but also on the previous outputs
- •Previous output is nothing but the present state
- •Therefore, sequential circuits contain combinational circuits along with memory storage elements
- •Some sequential circuits may not contain combinational circuits, but only memory elements



LATCH

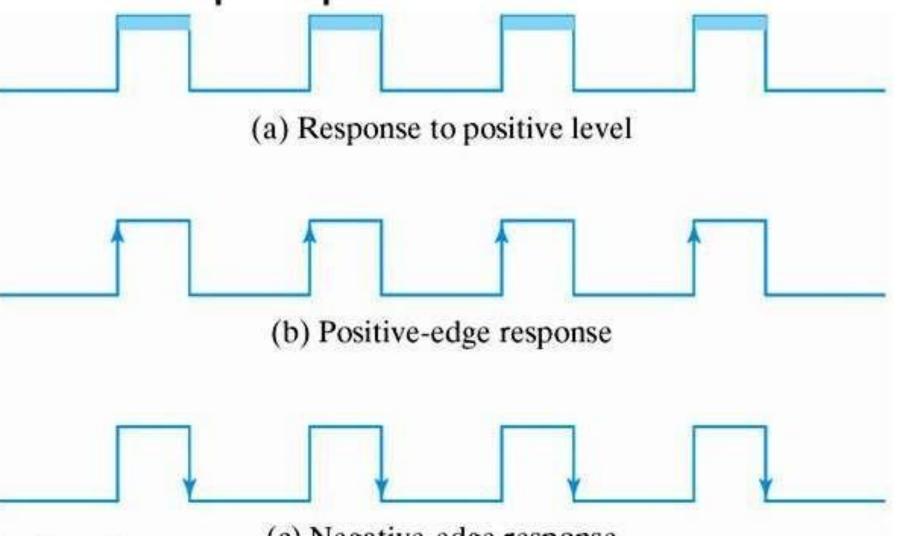


- LATCH –building block of sequential circuits capable of storing one bit information
- It has 2 output states Q and Q Complement
- It is built from Logic gates
- Latches does not have Clock signal instead it have enable line
- Output changes only when enable input signal is applied
- Latch is level Triggered





- A trigger
 - The state of a latch or flip-flop is switched by a change of the control input
- Level triggered latches
- Edge triggered flip-flops

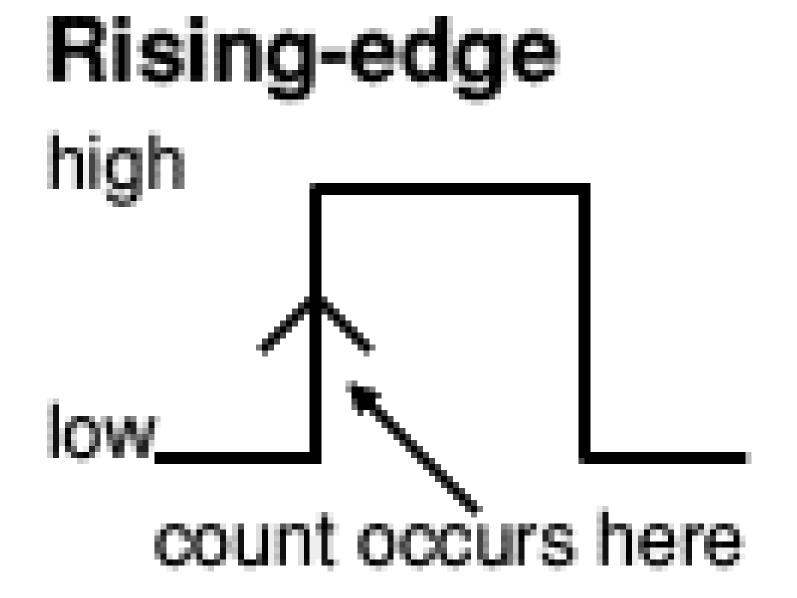


. 5.8



EDGE TRIGGERING





Falling-edge

count occurs here





Level Triggering

- 1. It is of two types
 - High level triggering
 - Low level triggering
- The latch or flip-flop circuits which change their outputs only corresponding to active high or low levels are called as level triggered latches or flip-flops.

Edge Triggering

- 1. It is of two types:
 - Positive edge triggering
 - Negative edge triggering
- 2. Those flip-flops which change their outputs only corresponding to the positive or negative edge of the clock input are called as edge triggered flip-flops.



TYPES OF LATCH



1.SR Latch

R=Reset and S=Set

2.D Latch

D means Delay

3.T Latch

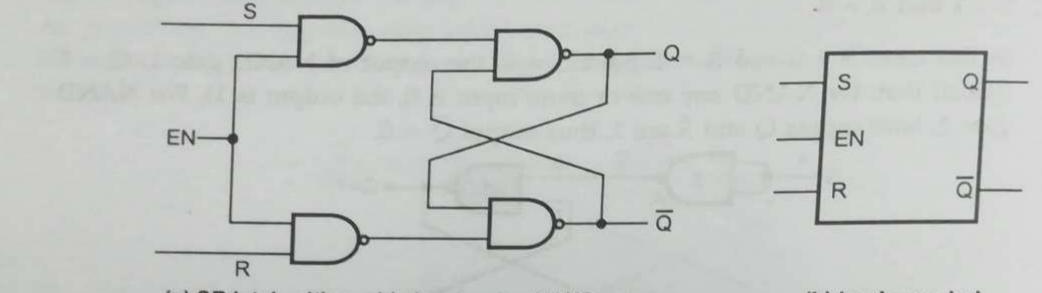
T means Toggle

4.JK Latch



SR LATCH





(a) SR latch with enable input using NAND gates

(b) Logic symbol

Fig. 6.7

EN	S	R	Qn	Qn+1	State
1	0	0	0	0	No change (NC)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	The state of the s
1	1	1	0	X	Indeterminate
1	1	1	1	X	
0	X	X	0	0	No change (NC)
0	×	X	1	1	

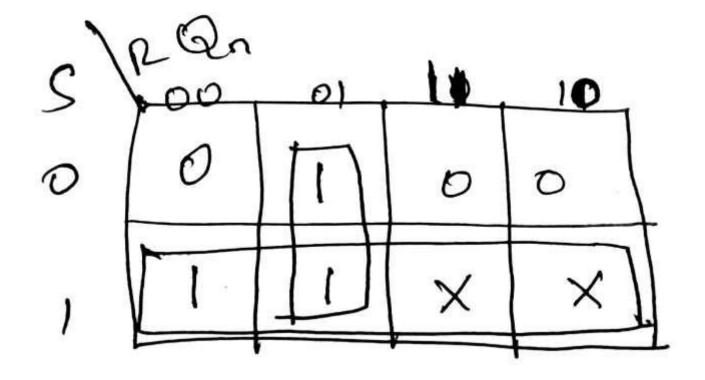
Table 6.2 Truth table for SR latch with enable input



SR LATCH



Characteristics Equation





SR LATCH



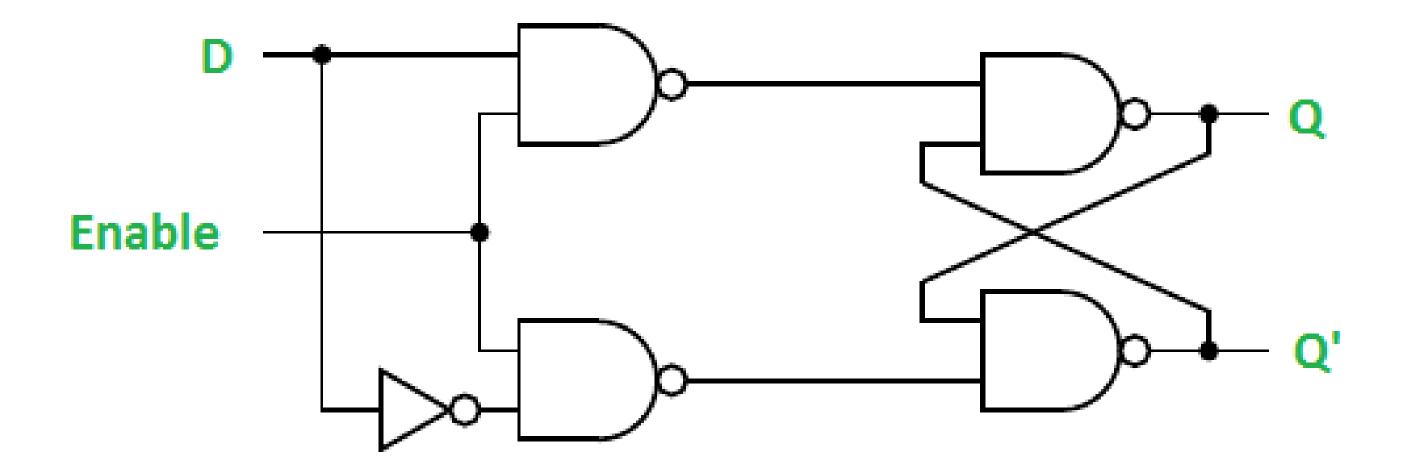
Excitation	Table

	Qr	9~	ک	R
1	0	0	0	\times
	0)	١	0
	1	10	0	, \
	l	1	X	0.



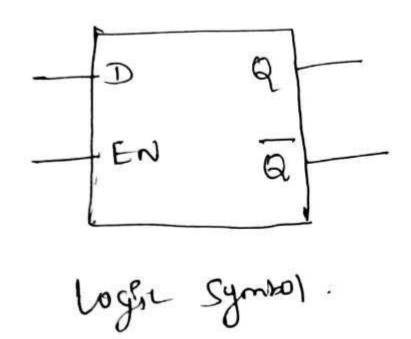
D LATCH

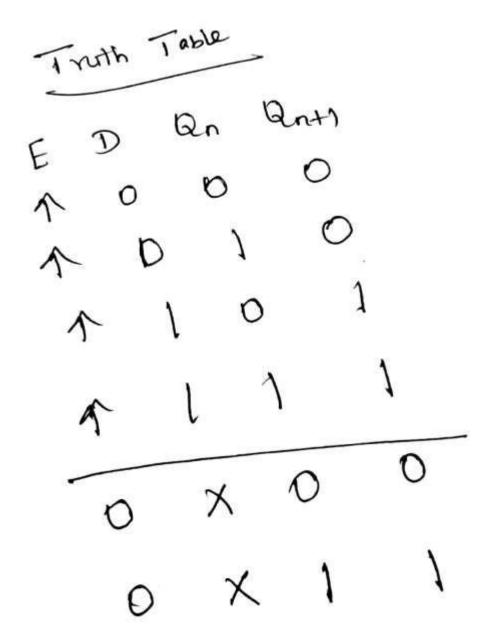








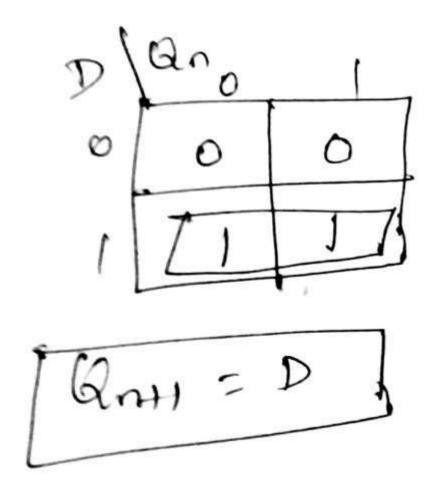








Characteristius Equation



Excitation table



ADVANTAGES OF LATCHES



- The advantages of latches include the following.
- The designing of latches is very flexible when we compare with FFs (flip-flops)
- The latches utilize less power.



APPLICATIONS OF LATCHES



- The applications of latches include the following.
- Generally, latches are used to keep the conditions of the bits to encode binary numbers
- Latches are single bit storage elements which are widely used in computing as well as data storage.



ASSESSMENTS



- 1.What is Latch?
- 2.List the types of latches.
- 3. Difference between level trigger and edge triggering.





THANK YOU