

SNS COLLEGE OF TECHNOLOGY

Coimbatore-35 An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB231 – DIGITAL ELECTRONICS

II YEAR/ III SEMESTER

UNIT 1 – MINIMIZATION TECHNIQUES AND LOGIC GATES

TOPIC 9– NAND-NOR IMPLEMENTATION







NAND and NOR implementation

> Any Boolean function can be created using AND OR and NOT gates.

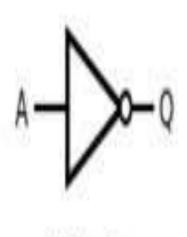
>AND, OR and NOT gates can be implemented using NAND and NOR gates.

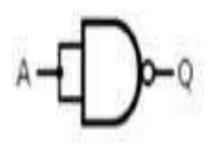


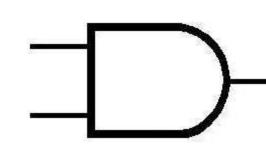


NAND implementation - Implementation of **NOT and AND using NAND gate**

A NAND gate with single input acts like a NOT gate. \triangleright As a NAND gate is the invert of AND so by putting an inverter on the output of NAND we can have AND gate.





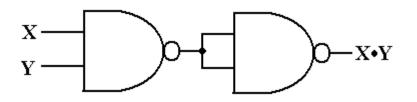


AND Gate

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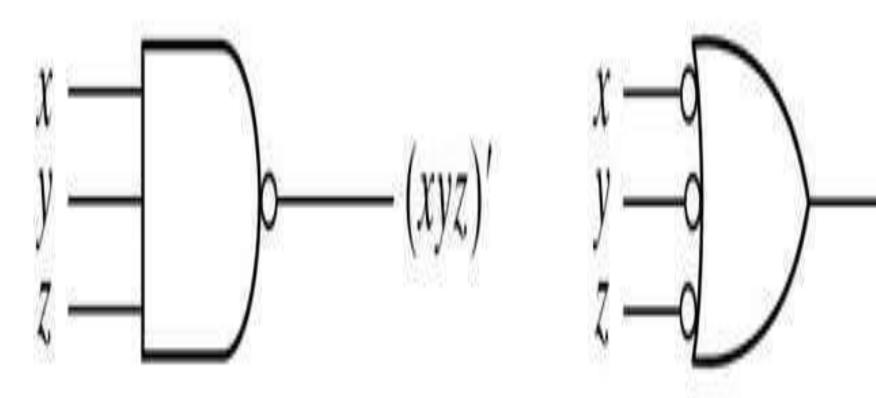




NAND Construction of ANDG ate



Symbolic Equivalence of NAND Gate



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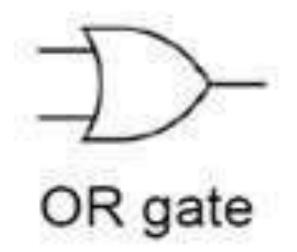


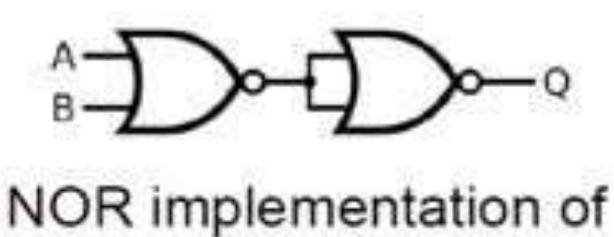
- x' + y' + z' = (xyz)'



NOR implementation - Implementation of OR gate using NOR gate

 \succ As NOR is the invert of OR gate so by putting an inverter in the output of NOR we get OR gate





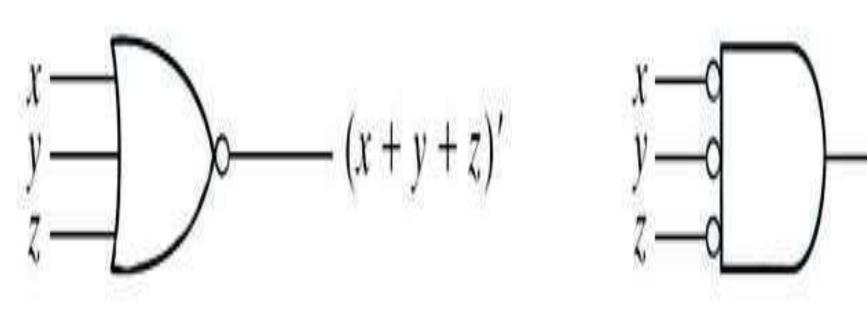
OR gate





Graphical equivalence of NOR gate

> By De Morgan's Law we can describe NOR gate graphically by the following symbols









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to DR moyany theorem)

+6+0

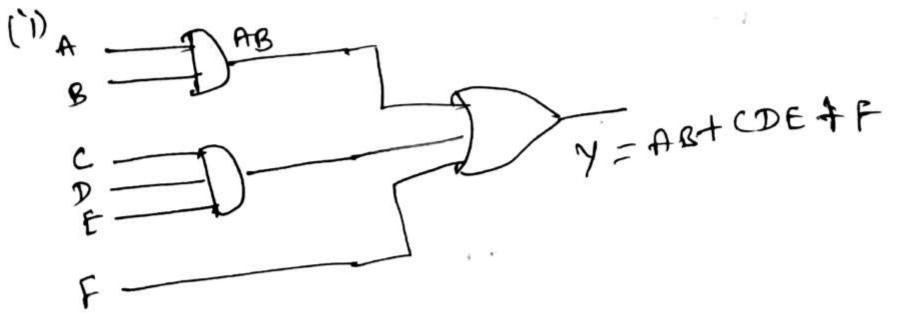
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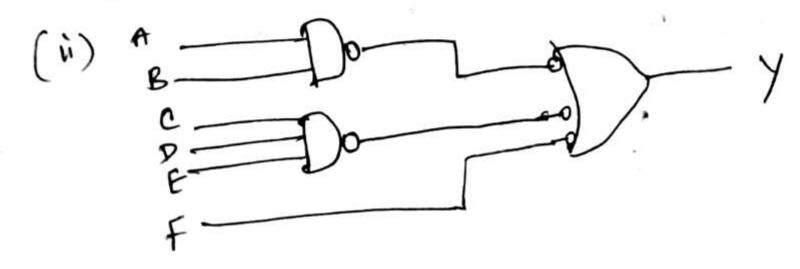
NAND invertary

NAND gates



Implement the following Boolean function wing only gates . Y = AB + CDE + F Lxample NAND gates



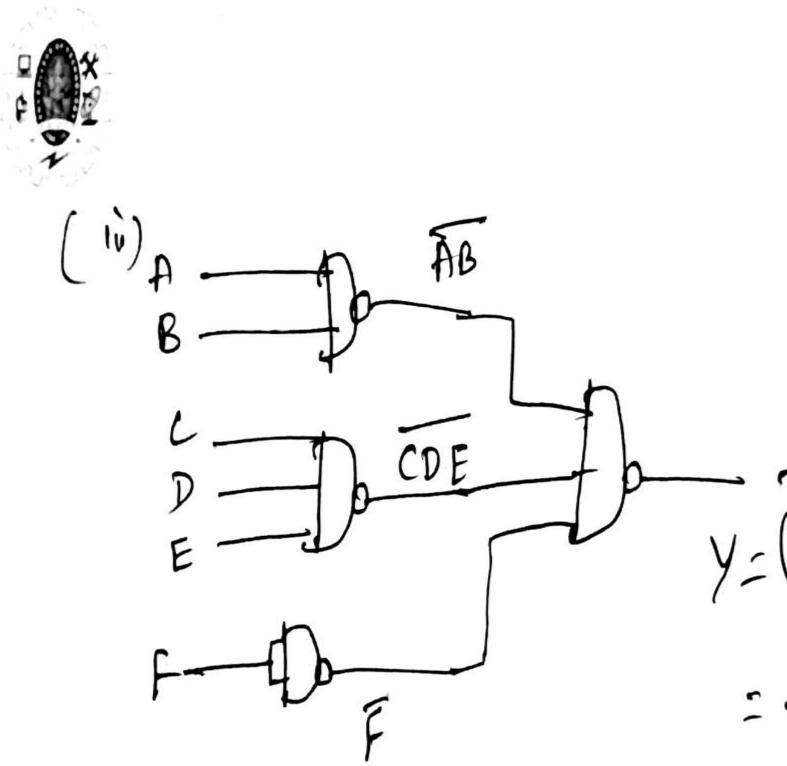


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 $Y = (\overline{AB})(\overline{CDE})(\overline{F})$

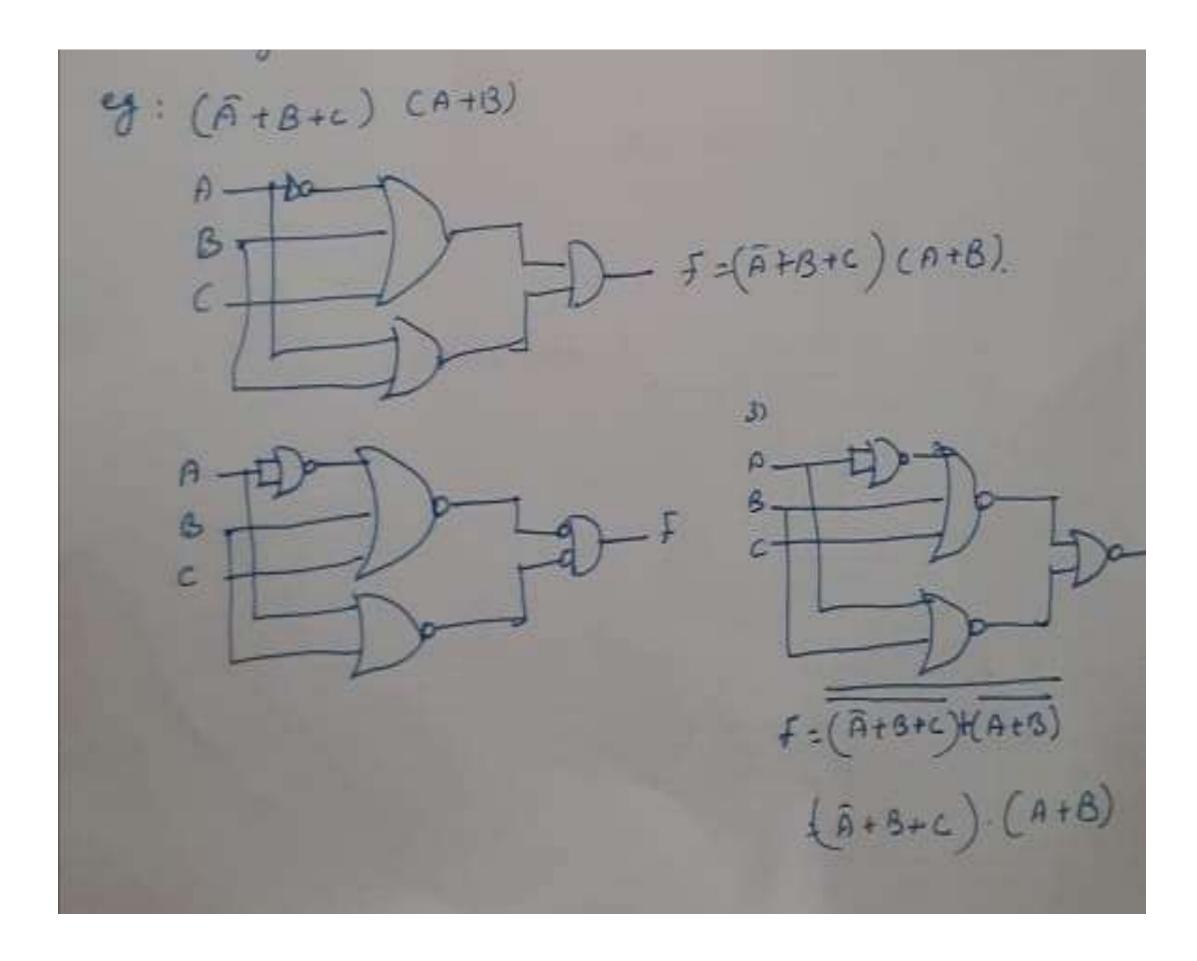
= AB+ (DE+F



NOR-NOR Implementation :-NOF = Bubbled AND A+B+C = ; (i) expression convert it into por fam procedure (ii) draw AND-OR-NOT redization (ii) arow HMD-UK-NUT reason (iii) Replace every OR gete by NOR, AND gate and inverter by a NOR invertey (ii) Finally, drew the final cirvuit M Only







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THANK YOU

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