Biasing Circuits for JFET

FET is a unipolar device where the conduction is only due to majority carriers. It is a voltage controlled device where I_D is a func of applied bias at gate.

Like BJT, parameters of FET are also temp dependent. In FET as temp ↑ drain resis also ↑ ⇒ ↓ I_D. Thus thermal runaway does not occur with FET.

In FET amp,

$$I_G = 0A$$

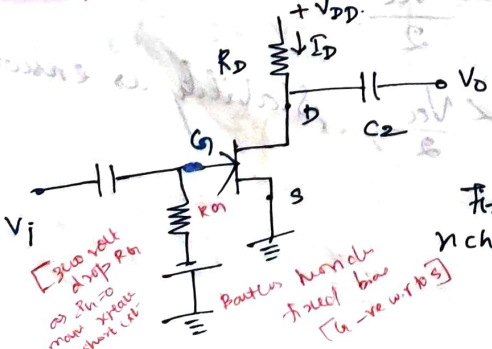
$$I_D = I_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \therefore V_P \Rightarrow \text{pinch off voltage}$$

Different biasing circuits of FET are,

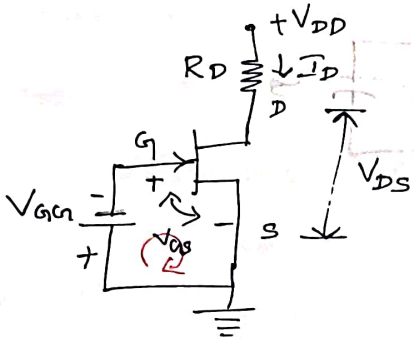
- fixed bias ckt
- self bias ckt
- voltage divider bias ckt

Fixed bias circuit. → fixed



Fixed bias ckt for n channel ckt JFET

For d.c. analysis coupling capacitors are open ckts. The I through R_G is I_G which is zero. So, R_G is replaced by short circuit, simplifies fixed bias ckt



Simplified fixed bias.

Step 1: Calculate V_{GS}

For D.C analysis, $I_G = 0$ & apply KVL to i/p ckt,

$$-V_{GG} - V_{GS} = 0$$

$$\therefore V_{GS} + V_{GG} = 0$$

$$\therefore V_{GS} = -V_{GG}$$

Step 2: Calculate I_{DQ} — shockley eqn

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Step 3: Calculate V_{DS}

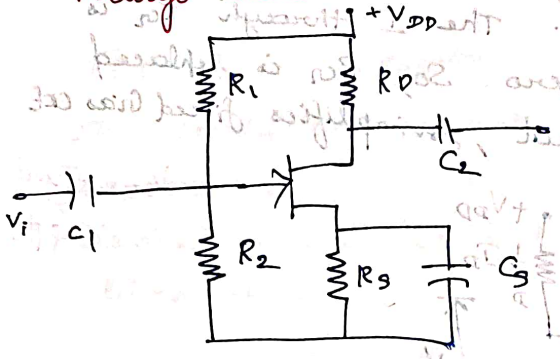
Apply KVL,

$$V_{DD} - I_D R_D - V_{DSQ} = 0$$

$$V_{DSQ} = V_{DD} - I_D R_D.$$

The main drawback of fixed bias ckt of FET is that it requires 2 power supplies

Voltage Divider bias circuit:

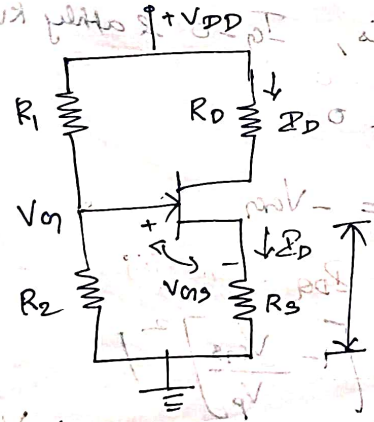


Source voltage,

$$V_S = I_D R_S$$

D.C. Analysis:

Simplified voltage divider circuit for dc analysis



Step 1: Calculate V_G.

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2} \quad \because I_G = 0$$

Step 2: Find V_{GS}.

Apply KVL to i/p ckt,

$$V_G - V_{GS} - I_D R_S = 0$$

$$V_{GS} = V_G - I_D R_S$$

Step 3: calculate I_{DQ}

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$ ✓

Step 4: Calculate V_{DS} & V_{GS}

Apply KVL to o/p ckt

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

The Q pt of JFET amp using the voltage divider bias is given by:

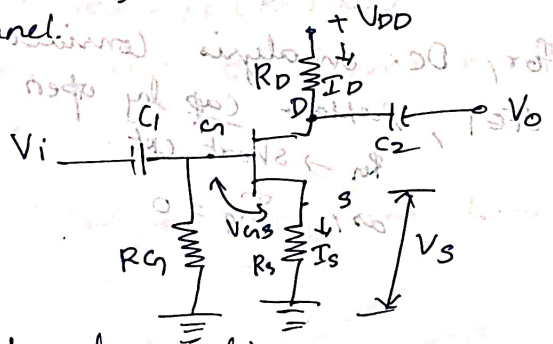
$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$V_{DSQ} = V_{DD} - I_D (R_D + R_S)$$

$$V_{GSQ} = V_G - I_D R_S$$ Pblm

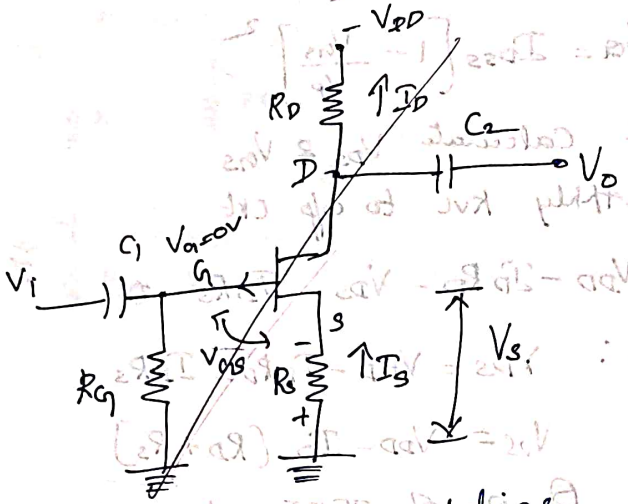
Self bias circuit – eliminates need for 2 DC supply

Self bias is the most common type of JFET bias. JFET must be operated such that the gate source junction is always reverse biased. This condition requires $-V_{GS}$ for n-channel & +ve V_{GS} for p-channel.



Now V_{GS} → controlling V_{GS} is determined by volt across R_S

a) n-channel self bias



P-channel self bias

DC analysis

Step 1 : V_{GS}.

$\boxed{I_S = I_D}$ & $V_G = 0$

For n-channel, $V_S = I_S R_S = I_D R_S$

Source -ve w.r. Gnd

$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$

For p-channel, source +ve w.r. Gnd

$V_S = -I_S R_S = -I_D R_S$

$V_{GS} = V_G - V_S = 0 - (-I_D R_S)$

$= I_D R_S$.

For, DC. analysis consider n-channel JFET, replace cap by open ckts.

$R_G \rightarrow$ short ckt.

as, $I_G = 0$

i) V_{GS}:

$V_{RS} = I_D R_S$

$-V_{GS} - V_{RS} = 0$

$\boxed{V_{GS} = -I_D R_S}$

ii) $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

$= I_{DSS}\left[1 + \frac{I_D R_S}{V_P}\right]^2$

iii) V_{DS}:

$V_{RS} + V_{DS} + I_D R_D - V_{DD} = 0$

$I_D = I_S$

$V_{DS} = V_{DD} - I_D(R_S + R_D)$

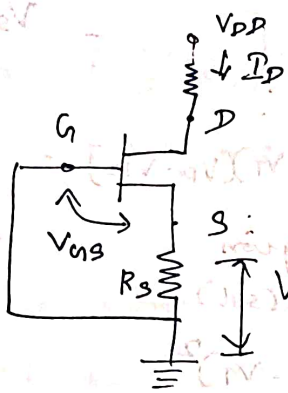
$\boxed{V_S = I_D R_S}$

$\boxed{V_G = 0V}$

$V_D = V_{DS} + V_S$

$= V_{DD} - V_{RD}$

Simplified self bias circuit for dc analysis



JFET | MOSFET
↓ ↓
only depletion mode | enhancement
↓
small leakage
↓
high i/p imp

I_{DQ}:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Sub $V_{GS} = -I_D R_S$ in above eqn

$$I_D = I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

$$= I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

Enhancement are off on $0 at V_{GS}$

dep on at $V_{GS}=0$ V_{GS}

V_{DS}:

Apply KVL to o/p ckt, $V_{DD} - I_D R_D - V_{DS} - V_S = 0$

$$V_S + V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - V_S - I_D R_D$$

$$= V_{DD} - I_D R_S - I_D R_D$$

$$= V_{DD} - I_D (R_S + R_D)$$

$V_{DD} = I_D R_D + V_{DS} + V_S$

$V_{DD} - I_D R_D$ V_{DS}

Pblms on design of biasing for JFET.

Biasing of MOSFET:

The ideal current voltage equations are,