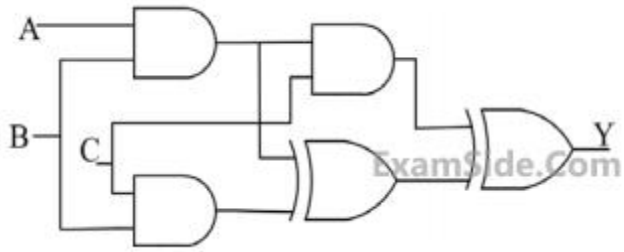
GATE ECE 2016 Set 1

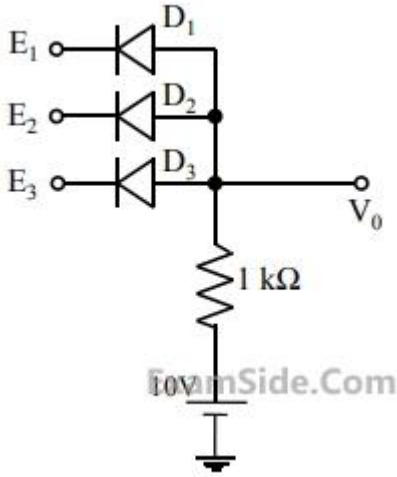
1. The output of the combinational circuit given below is



A
A+B+C
B
A(B+C)
C
B(C+A)
D
C(A+B)

GATE ECE 2015 Set 3

2. In the circuit shown, diodes D_1D1 ,D_2D2 and D_3D3 are ideal, and the inputs E_1E1 , E_2E2 and E_3E3 are “0 V” for logic ‘0’ and “10 V” for logic ‘1’. What logic gate does

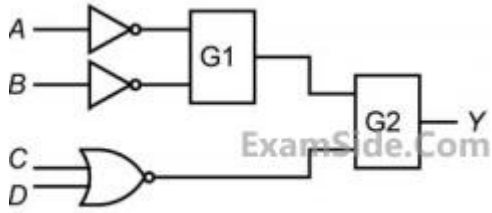


the circuit represent?

A
3-input OR gate
B
3-input NOR gate
C
3-input AND gate
D
3-input XOR gate

3. GATE ECE 2015 Set 2

In the figure shown, the output is required to be Y=AB+ $\overline{CC}\,\overline{DD}$. The gates G1 and G2 must be,



respectively,

A
NOR, OR

B
OR, NAND

C
NAND, OR

D
AND, NAND

GATE ECE 2013

4. A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles.

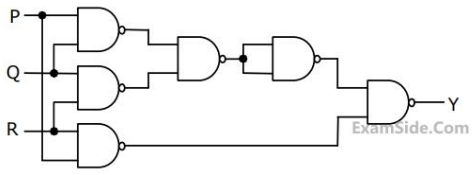
A
an AND gate

B
an OR gate

C
an XOR gate

D
a NAND gate

5. GATE ECE 2011

The output Y in the circuit be 

low is always '1' when

A

two or more of the inputs P, Q, R are ‘0’

B

two or more of the inputs P, Q, R are ‘1

C

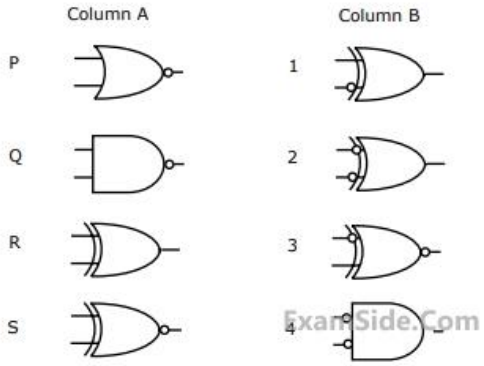
any odd number of the inputs P, Q, R is ‘0’

D

any odd number of the inputs P, Q, R is ‘1’

6. GATE ECE 2010

Match the logic gates in column A with their equivalents in column B.



A

P-2, Q-4, R-1, S-3

B

P-4, Q-2, R-1, S-3

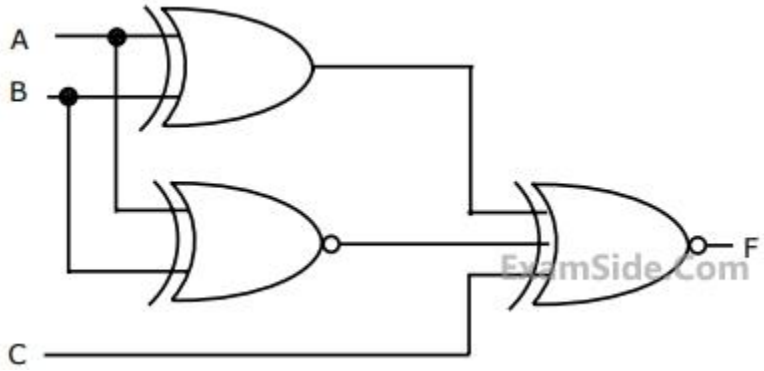
C

P-2, Q-4, R-3, S-1

D

P-4, Q-2, R-3, S-1

7. For the output F to be 1 in the logic circuit shown, the input combination should be



A

A = 1, B= 1. C = 0

B

A = 1, B= 0,C = 0

C

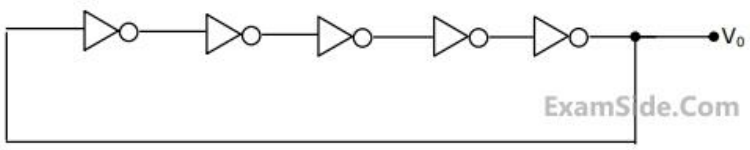
A = 0, B= 1. C = 0

D

A = 0, B= 0, C = 1

8. GATE ECE 2001

For the ring oscillator shown in the figure, the propagation delay of each inverter is 100 pico sec. What is the fundamental frequency of the oscillator output?



A

10 MHz

B

100 MHz

C

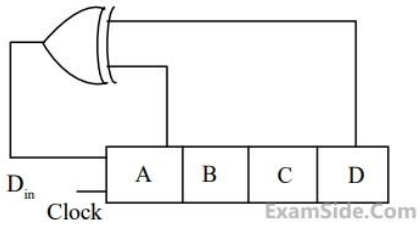
1 GHz

D

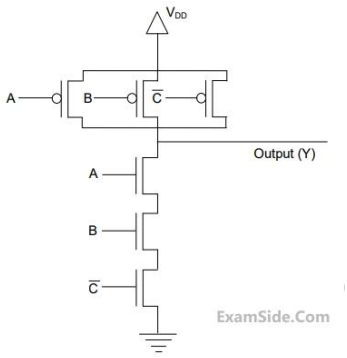
2 GHz

9. GATE ECE 2017 Set 1

A 4-bit shift register circuit configured for right-shift operation is $D_{in} \rightarrow A, A \rightarrow B, B \rightarrow C, C \rightarrow D$, $Din \rightarrow A, A \rightarrow B, B \rightarrow C, C \rightarrow D$, is shown. If the present state of the shift register is ABCD = 1101, the number of clock cycles required to reach the state ABCD = 1111 is



10. GATE ECE 2014 Set 4



The output (Y) of the circuit shown in the figure is

A

$\overline{A}+\overline{B}+\overline{CA}\overline{B}\overline{C}$

B

$A+\overline{B}.C+A.\overline{CA}+B\overline{.C}+A.C$

C

$\overline{A}+B+\overline{CA}\overline{B}\overline{C}$

D

$A.B.\overline{CA}.B.C$